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13. ABSTRACT (Maximum 200 words)

The indium phosphide-based SLED is an ideal light source for eye-safe target designation and imaging at 1550 nm spectral region. Its wide spectral width ensures low coherency, which is critical for speckle free imaging. A high brightness and well-collimated output beam allow for projection of the illumination across long distances.

In this project, a high brightness SLED chip that exceeds 200 mW in peak optical power output and >20 nm of spectral bandwidth at 1550 nm wavelength has been designed, developed and demonstrated. This optical power level is the highest value ever achieved, exhibiting more than 2 times improvement over baseline SLED chips operating in the same wavelength range.

The SLED chip is packaged into a compact 7-pin TO-8 platform with built-in collimating aspherical lens, and the resultant transmitter optical sub-assembly (TOSA) achieved a very low beam divergence of 1 mrad. Additionally, an optical pulse stream of 10 ns pulse width, 0.1% duty ratio and rise and fall times of 1 ns has been demonstrated, allowing for high speed pulsed illumination applications.

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Enclosure 1

Speckle Free, Low Coherency, High Brightness, and High Pulse Speed Infrared Collimated Light Sources for Mid-IR Target Designator and Hyperspectral Imaging

DARPA Project No. 50728-PH-DRP

Final Report

Submitted by DenseLight Semiconductors Pte Ltd

Date: 31 Oct 2007

DenseLight Semiconductors

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1. Introduction

1.1 Overview of Project

1.1.1 Laser guidance is used extensively in the modern battlefield on multiple weapon systems ranging from rockets to missiles to guided bombs. The guidance scheme relies on a laser designator to illuminate a target with reflected light, and the weapon system will contain a seeker for homing in on the energy reflected from the target. The traditional target designator operates in the 1064 nm spectral band, with pulsed light source of the solid-state Nd:YAG laser.

1.1.2 These illuminators need to have high brightness and speckle free output beam. Additionally, these need to be capable of being modulated with high-speed electrical pulse train to generate high levels of peak optical power, to work in conjunction with electronic gating function of associated equipment. Furthermore, there is a need for built-in collimating optics to provide a low divergence output light beam. With the proliferation of use of such equipment in the field, there is an urgent need to develop designators and illuminators in the "eye-safe" spectral region of around 1550 nm.

1.1.3 The Superluminescent LED (SLED) technology is ideally suited to fulfill the above requirements. It is a broadband incoherent light source with Gaussian beam profile, which allows for speckle-free imaging and good collimation to a low divergence. In this project, the SLED chip will be designed for high output power, broadband spectral output and high-speed modulation capability, along with the development of a matching opto-mechanical package containing collimating optics. Another goal in this effort is to explore SLED designs to improve the power efficiency, as high efficiency sources are critical for field operations.

1.1.4 Design of the SLED light source will target it to be rugged, tolerant of harsh operating environments and field installable. By incorporating DFX concepts and methodology in the development project right from the beginning, the developed optical component will be able to be subsequently manufactured in volume, and pressed into service for the warfighter in a timely manner.

1.1.5 Vision of this current effort extends well beyond the initial application for eye-safe target designators. The SLED core platform will be developed in the initial exploratory phase so as to be scalable. Subsequent effort in follow-on phase projects could expand the range of wavelength output and beam collimation. This will result in a complete suite of illuminator elements covering a wide range of wavelengths and collimation optics. This will pave the way for providing the source of illumination suitable for hyperspectral imaging systems. A customized combination of illuminator elements can thus be selected to suit the profile of each mission and requirement.

1.2 Organization of Project

1.2.1 This 12-month project is organized into three concurrent development efforts in

a) *SLED chip design and fabrication development*
For this part, SLED chip is developed to meet target performance, specifically that of output power and power efficiency.

b) *Package design and assembly development*
Here, development of the SLED package is performed to achieve good optical collimation and supporting high speed pulse output.

c) *Device test development*
The test methodology and test setup of SLED chip and package are also developed to characterize the fabricated SLED chip and assembled SLED modules.

1.3 Target Performance

1.3.1 The target performance of the speckle free, low coherency and high brightness SLED module is tabulated as follows:

	Parameter	Specs
SLED Device	Center wavelength	1550 ± 15nm
	Spectral width (3dB)	20 to 30nm
	Modulation rise and fall time	1ns
	Pulsed output power*	> 0.2W (from package)
	Output far field	nearly circular
	Chip power efficiency (PE)	20%
Packaging Platform	Miniature footprint (TO-8, or equivalent, form factor)	
	Hermetically sealed operation	
	Internal TEC (thermoelectric cooler) for operation over case temperature range of –40 to +40°C	
	Integral collimating optics to produce output beam divergence of < 2mrad	
	Control of RLC parasitics to support high-speed modulation	

* ~15ns pulse width with 100kHz rep rate

2. SLED Chip Design and Fabrication Development

2.1 Organization of Design Stages

2.1.1 The SLED chip design and fabrication development is organized into three stages, as shown in Fig. 2-1.

DS01 (Power-BW tuning):

This first stage involves increasing the optical gain by increasing quantum well (QW) number, optimizing QW design and ridge waveguide structure, to realize optical power of >130 mW.

DS02 (Power-BW tuning):

In this next stage, the optical power is to be further ramped up by also increasing the number of QW and optimizing the QW design.

DS03 (Power-BW-PE-Far field optimization):

The design strategy in this third stage is to i) increase optical gain by increasing device length, ii) reduce optical loss by optimizing doping profile and waveguide structure, iii) reduce voltage drop by optimizing doping profile to reduce series resistance and iv) tune refractive index profile by optimizing waveguide epi-layer design.

DS04 (Advanced FF refinement):

The optical far-field mode profile of the SLED chip will be fine-tuned to best match the collimation optics so as to realize beam divergence of <2 mrad for the packaged TOSA module.

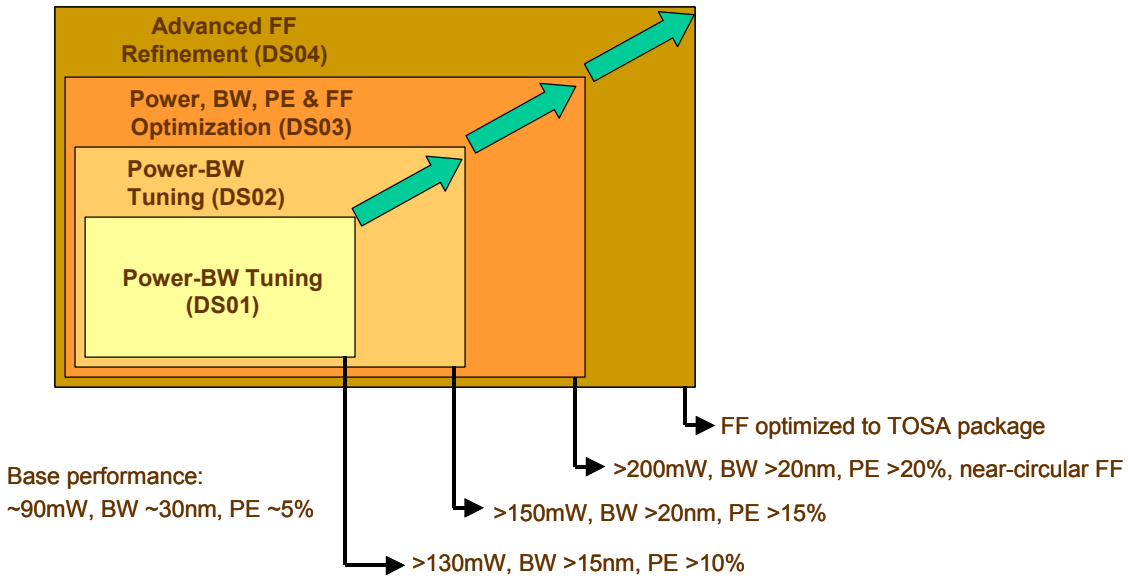


Figure 2-1: SLED chip design and fabrication development organization chart

2.2 SLED Chip Design

2.2.1 Several design and simulation methodologies have been adopted in the SLED chip design, including:

(i) Computing optical parameters, such as gain coefficient, spontaneous emission coefficient, Auger recombination coefficient and optical confinement factors using Advanced Laser Diode Simulator (ALDS) from Apollo Photonics

(ii) Modeling optical modes of light propagation along SLED waveguide using Beam Propagation Method (BPM) from Optiwave

(iii) Solving carrier density using rate equations

(iv) Computing electrical parameters independently from material constants and device parameters

2.2.2 A few assumptions have been made in the SLED design, and they are

(i) Facet reflectivity is negligible

(ii) Waveguide structure variations along device length is not considered

(iii) Uniform carrier density across length of SLED

(iv) Higher order effects (e.g. scattering from defects & sidewalls, index variation from carrier density variations) are ignored

2.2.3 In consideration of implementation of the design, optimization of other device parameters to maintain optical confinement and lasing suppression, as well as tuning of fabrication process conditions were also carried out. Table 2.1 shows the summary of design strategies adopted in the various development stages.

Table 2-1: Chip design development stages, strategies and action

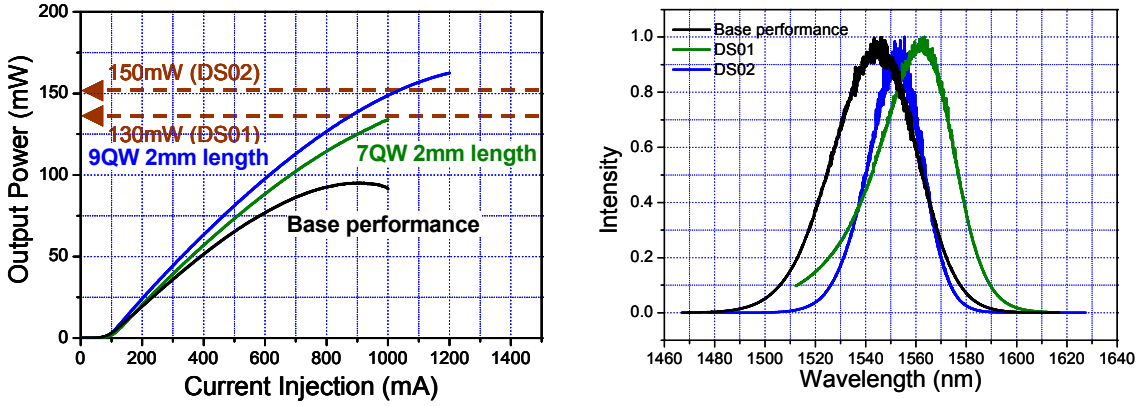
Development Stage		Design Strategy	Proposed Action
DS01	Power-BW Tuning	• Increase optical gain	• Increase QW number • Optimize QW design • Optimize ridge waveguide structure
DS02	Power-BW Tuning	• Increase optical gain	• Increase QW number • Optimize QW design
DS03	Power, BW, PE & FF Optimization	• Increase optical gain	• Increase device length
		• Reduce optical loss	• Optimize doping profile • Optimize waveguide structure
		• Reduce voltage drop	• Optimize doping profile to reduce series resistance
		• Design refractive index profile	• Optimize waveguide epi-layer design
DS04	Advanced FF Refinement	• Further modification to match FF to desired profile	• Fine-tune QW and confinement layer design

2.3 Process and Outcome

Power-BW Tuning (DS01 and DS02)

2.3.1 The base design of the SLED chip is based on 5 quantum wells, whereby an optical power of 90 mW has been obtained. For the design stages of DS01 and DS02, the number of quantum wells in the active region is increased to 7 and 9 respectively. The SLED device length is also increased from 1.5 mm to 2 mm in both DS01 and DS02.

2.3.2 Figure 2-2 shows the measured performance of SLED fabricated based on designs of DS01 and DS02. The SLEDs are characterized at chip-on-submount (CoS) level with optical power obtained using Keithley L-I-V tester and optical spectrum captured using ANDO A6317B optical spectrum analyzer (OSA).



(a) (b)

Figure 2-2: Optical performance of DS01 and DS02 SLED
(a) Optical power vs current injection, and (b) Optical spectrum

2.3.3 A higher optical gain achieved via a larger number of quantum well and longer device length resulted in high optical powers of 130 and 150 mW at 1 A current injection for DS01 and DS02 designs respectively. The optical spectrum 3dB bandwidth is maintained around 22 to 32 nm in both stages, demonstrating that incoherency has not been affected by the higher optical power. Comparison of the simulation and experimental results is shown in Fig. 2-3. The optical power measured from the SLED devices in both stages are close to the simulated power. Figure 2-4 illustrates the optical far field of the SLED CoS measured using Photon Inc Goniometric Radiometer. Near-circular far field has been obtained from the SLEDs.

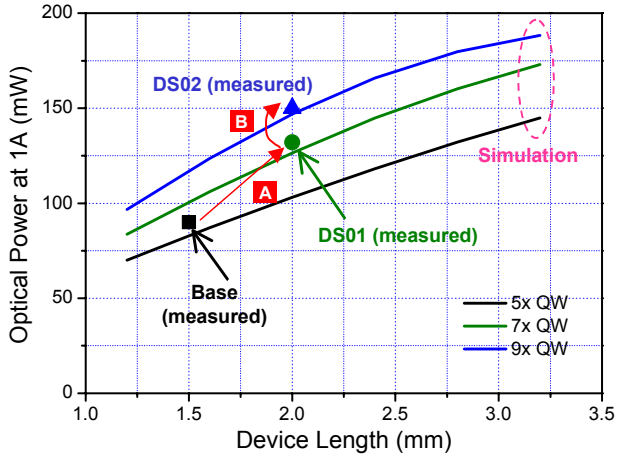
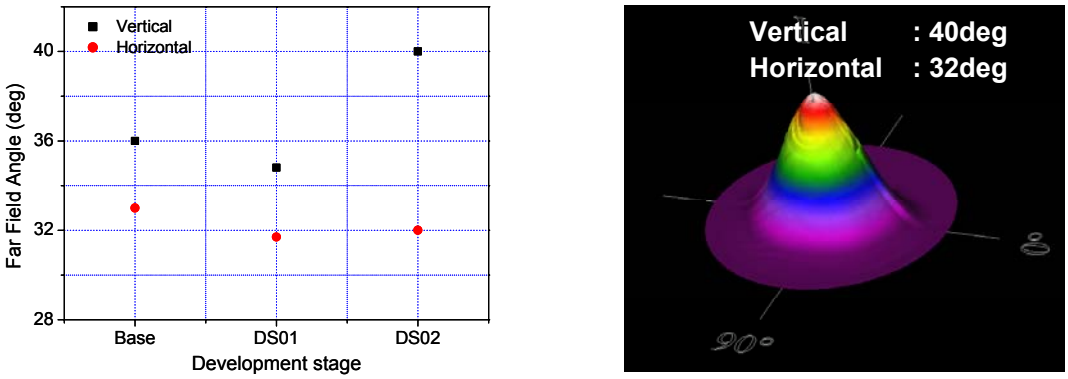


Figure 2-3: Comparison between simulation and experimental results of DS01 and DS02



(a) (b)

Figure 2-4: (a) Comparison of optical far field angles, (b) 3D Optical far field profile for DS02

Power, BW, PE & FF Optimization (DS03)

2.3.4 To further push up the optical power output and also the power efficiency of the SLED, the device length is increased from 2 mm (DS02) to 3 mm. In addition, the doping profile of the SLED PIN diode is optimized to realize lower internal optical loss. This is implemented with the introduction of a new InP buffer layer directly above the active waveguide that has a lower p-type doping (high p-type doping is known to result in higher optical loss), as shown in Fig. 2-5.

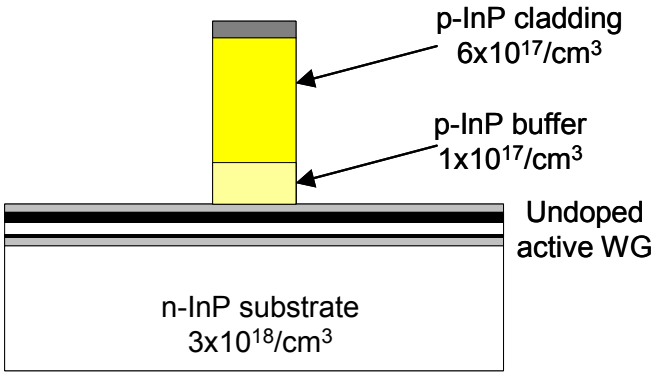


Figure 2-5: Optimization of doping profile with lighter doping p-InP buffer

2.3.5 Figure 2-6 shows the dependence of the absorption loss and bulk resistance of the SLED ridge waveguide with respect to the p-InP buffer thickness based on the 7QW structure design. It can be clearly seen that the absorption loss drops exponentially with the p-InP buffer thickness, but a thicker p-InP buffer layer also leads to an increase in the bulk resistance. Hence, there is a need to optimize the p-InP buffer layer thickness to realize the best SLED performance, and this is projected to be around 150 nm with an estimated power efficiency of 20%.

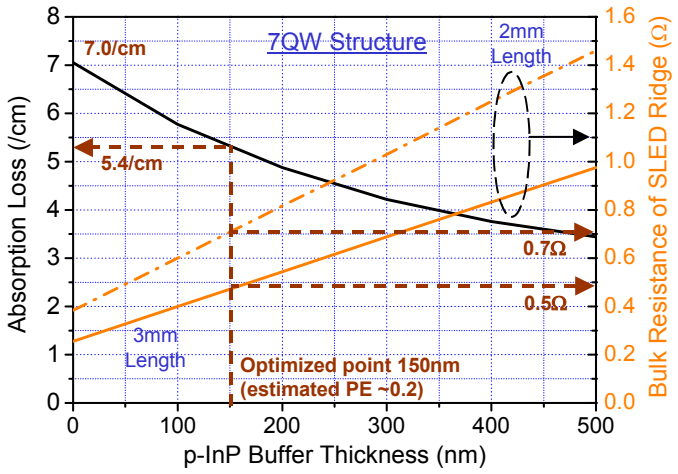


Figure 2-6: Absorption loss and bulk resistance of ridge vs p-InP buffer thickness

2.3.6 The four designs of DS03-A to D are outlined in the following Table 2-2. Figure 2-7 shows the expected optical powers at 1 A for the four respective designs. The estimated power for the best DS03-D design (with 9QW, 3 mm device length and doping optimization) is ~290 mW.

Table 2-2: Design optimization implemented in DS03

DS03-A	7QW @2mm (130mW) DS01	Doping Opt ⇒	7QW @2mm Doping Opt (T: 170mW)
DS03-B	9QW @2mm (150mW) DS02	Length ↑ ⇒	9QW @3mm (T: 185mW)
DS03-C	9QW @2mm (150mW) DS02	Doping Opt ⇒	9QW @2mm Doping Opt (T: 200mW)
DS03-D	9QW @2mm Doping Opt (T: 200mW)	Length ↑ ⇒	9QW @3mm Doping Opt (T: 290mW)

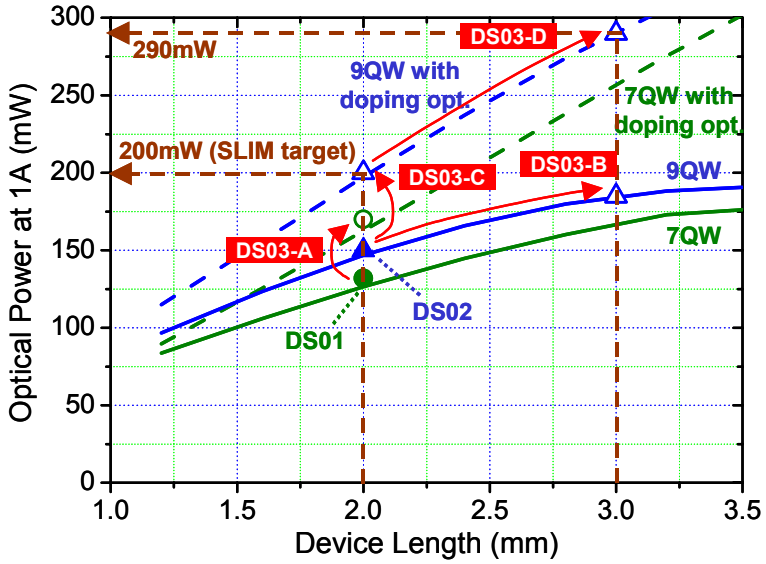


Figure 2-7: Optical power vs device length with various optimization scheme

2.3.7 Four wafer runs were carried out for the designs DS03-A to D. The measured peak optical powers for DS03-A and C are shown in Fig. 2-8. A peak optical power of 220 mW is achieved for a current injection of 1.4 A. As explained in Table 2-3, when compared to DS02, the result of DS03-A demonstrates that the doping optimization design roughly compensates for 2 fewer quantum wells in DS03-A. In addition, it can also be observed that a lower realized strain for DS03-C sample leads to a lower overall optical gain.

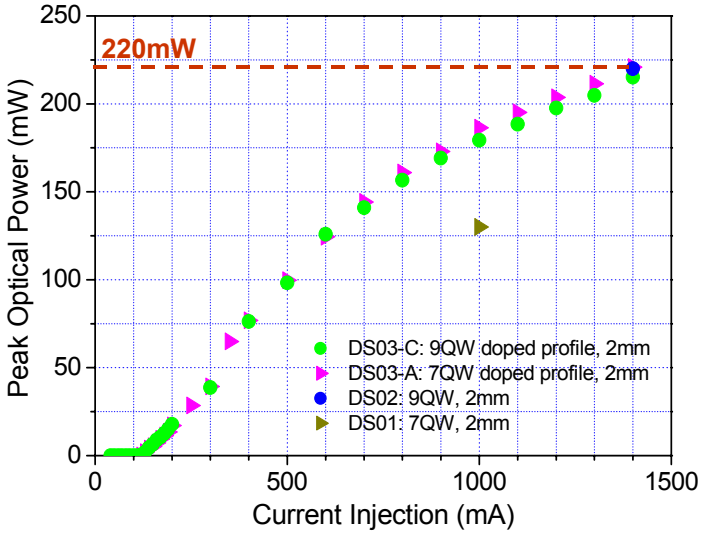


Figure 2-8: Measured peak optical power performance of DS01, DS02, DS03-A and DS03-C

Table 2-3: Comparison and analysis of SLED chip designs DS02 and DS03

ID	SLED Design Parameters (QW #, Length)	Measured Growth Strain	Measured LI	Observations
DS02	9QW, 2mm	1.0%	220mW at 1.4A	Reference
DS03-A	7QW, 2mm, Doping Optimization	1.1%	221mW at 1.4A	Doping roughly compensates for 2 fewer QW
DS03-C	9QW, 2mm, Doping Optimization	0.8%	215mW at 1.4A	Smaller 9QW-strain lowers overall optical gain

2.3.8 The power efficiency (PE) attained in DS03-A is 10% at 1A current drive, as shown in Fig. 2-9. The PE peaks at 14% at 400 mA drive and subsequently drops to 7% at 1.4 A current. Further increase of PE requires a longer device length of 3mm to get higher optical power at higher current with minimal increase in the operating voltage, as described in Table 2-4.

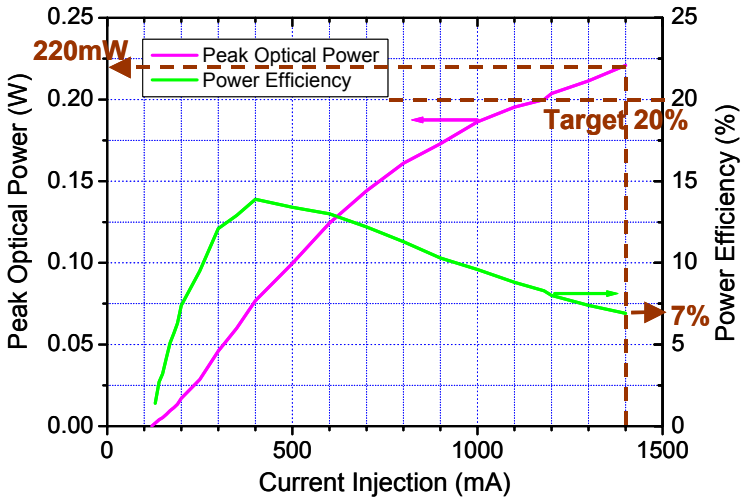


Figure 2-9: Power efficiency of SLED chip of design DS03-A

Table 2-4: Comparison of SLED chip designs for higher PE

ID	SLED Design Parameters (QW #, Length)	Projected Optical Power at 1A	Projected Voltage Drop at 1A	Projected Power Efficiency at 1A
DS03-A'	7QW, 3mm, Doping Optimization	220 ~ 240mW	1.78V	12 ~ 13%
DS03-D	9QW, 3mm, Doping Optimization	260 ~ 280mW	1.78V	15 ~ 16%

2.3.9 Four wafer runs each have been carried for designs DS03-A' (7QW, 3 mm, doping optimization) and DS03-D (9QW, 3 mm, doping optimization), as tabulated in Table 2-5. As shown in Fig. 2-10, we have been unsuccessful in getting good SLED chips of 3mm in length of DS03-A' and DS03-D; the optical power measured at 1 A is at most ~120 mW, well below the projected optical power values. Even with much process tuning for samples of DS03-A'-4 and DS03-D-4, the measured CW optical power is ~120 mW. We believe that this is due to the high built-in strain in the SLED chip, which affected the crystal quality and hence the optical performance.

Table 2-5: Wafer runs for 3mm SLED devices

ID	SLED Design Parameters (QW #, Length)	Wafer ID	Design Target P_{out} @1A	Measured P_{out} @1A	Status/Outcome
DS03-A'-1	7QW, 3mm	417006	255mW	<60mW	Fail to meet specs
DS03-A'-2	7QW, 3mm	417036	255mW	<100mW	Fail to meet specs
DS03-A'-3	7QW, 3mm	417042	255mW	<100mW	Fail to meet specs
DS03-A'-4	7QW, 3mm	417074	255mW	~120mW	Fail to meet specs
DS03-D-1	9QW, 3mm	417007	290mW	<60mW	Fail to meet specs
DS03-D-2	9QW, 3mm	417043	290mW	<100mW	Fail to meet specs
DS03-D-3	9QW, 3mm	417055	290mW	<100mW	Fail to meet specs
DS03-D-4	9QW, 3mm	417075	290mW	~120mW	Fail to meet specs

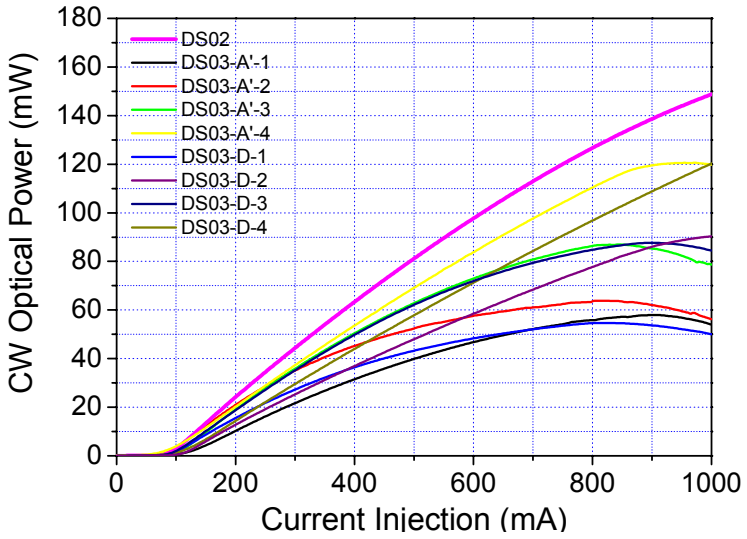


Figure 2-10: Optical power vs current injection of DS03-A' and DS03-D SLED samples

Advanced FF Refinement (DS04)

2.3.10 The optical far-field angles obtained for SLED chip of DS03-A design is 38º vertical versus 32º horizontal, which is near circular. Since this SLED chip can be matched with DP04 aspherical lens in the TOSA module to realize a beam divergence of <2 mrad (see section 3.4), this planned DS04 stage to further fine-tune the optical far-field of the SLED chip is skipped.

2.4 Summary

2.4.1 In this SLED chip development effort, the optical power of the SLED chip has been increased from the baseline value of 90 mW by 2.4× to 220 mW. This has been realized by increasing the number of quantum wells in the active region, increasing the device length to 2 mm and optimization the doping profile of the SLED diode structure. The

power efficiency has also been doubled from 5% to 10%. A near-circular optical far-field mode profile has also been obtained, which is expected to allow for good collimation to realize low beam divergence at the TOSA level.

3. Package Design and Assembly Development

3.1 Organization of Design Stages

3.1.1 The SLED package design and assembly development is divided into four stages, as shown in Fig. 3-1:

DP01 (TO-header sub-assembly development):

This development stage targets the assembly and integration of chip-on-submount (COS) and TEC unit or CuW block onto the TO-header. The completed sub-assembly can be used as a partially completed package for CW and pulse testing and also as starting material for DP02 capping development.

DP02 (TO-header capping development):

The main focus of this stage is to develop the hermetic sealed TO capping process. The capped TO-can will be subsequently be used for TOSA assembly.

DP03 (TOSA assembly development):

In this stage, the capped TO can is integrated with collimating lens to form the TOSA module. The key parameter of beam divergence is targeted to be <10 mrad.

DP04 (TOSA assembly optimization):

Optimization of the TOSA process, including the selection of longer focal length lens or spatial filter, is to be carried out to achieve final target beam divergence of <2 mrad.

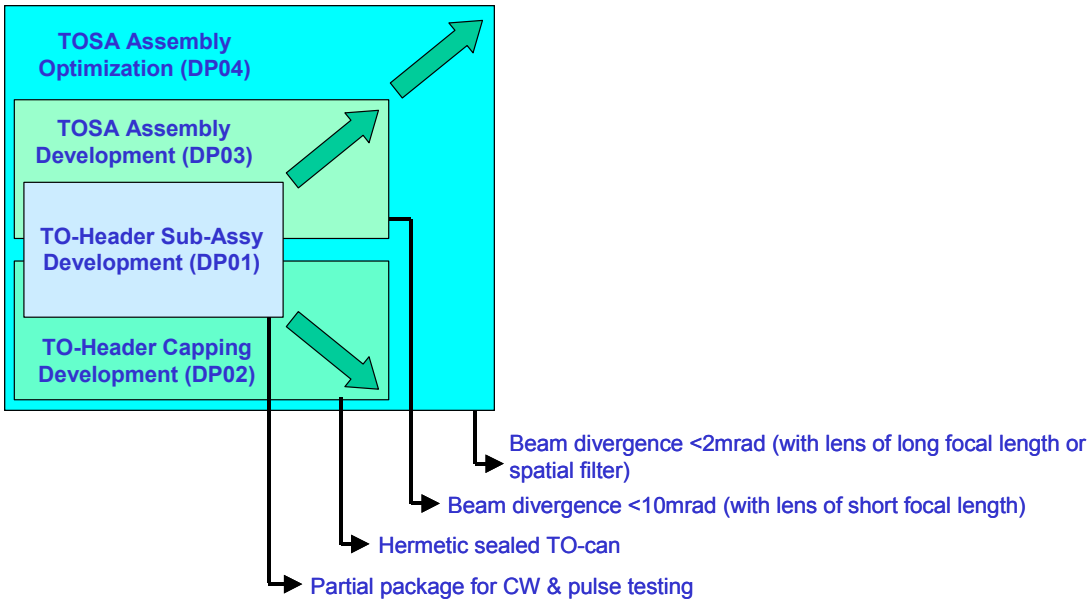
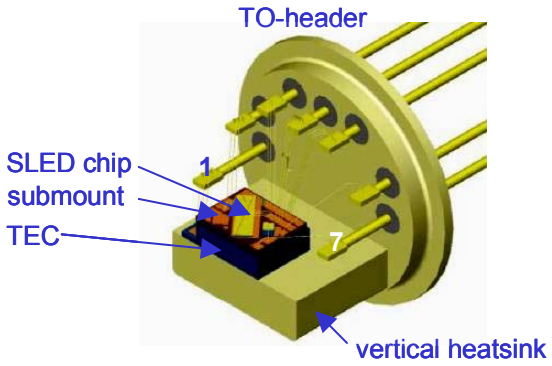


Figure 3-1: Package design and assembly development organization chart

3.2 TO-Header Sub-Assembly Development (DP01)

3.2.1 *Design*

3.2.1.1 The key consideration in the design of TO-can header, is its size, such that it could accommodate the SLED chip of at least 3mm in device length on the submount, the TEC unit, as well as allow for the vertical heatsink for COS-TEC mounting. At least 7 leads are needed to cater for the temperature sensing thermistor (×2), SLED cathode (×1), SLED anode (×1) and TEC unit (×2), together with one spare pin. The nearest available industrial form-factor standard for the can outline is TO-8 with diameter of >12 mm. This platform is also able to serve as the base-module for the collimation optical sub-assembly to be built upon. Figure 3-2 shows the configuration of the selected TO-8 header with vertical heatsink and 7 leads.



Pin Assignment	
1	TEC (+)
2	TEC (-)
3	SLED Cathode (-)
4	SLED Anode (+)
5	SLED Cathode (-)
6	Thermistor
7	Thermistor

Figure 3-2: TO-8 header with pin assignment

3.2.2 *Process Development and Results*

3.2.2.1 Figure 3-3 shows the process flow for fabrication of the TO-header sub-assembly. The process comprises integrating COS, TEC and the TO-header, and wire bonding from the respective pads to the leads of the header. A TO jig holder of Fig. 3-4 has been designed and fabricated to hold the TO header during this TO-header assembly process. The mounting of the CoS on TEC and then the COS-TEC on the TO header is carried out using a die-attach machine. The tolerance of the COS-TEC-header mounting process is +/-0.02 mm. The wire bonding of electrodes to the leads of the header is performed with 1 mil gold wires.

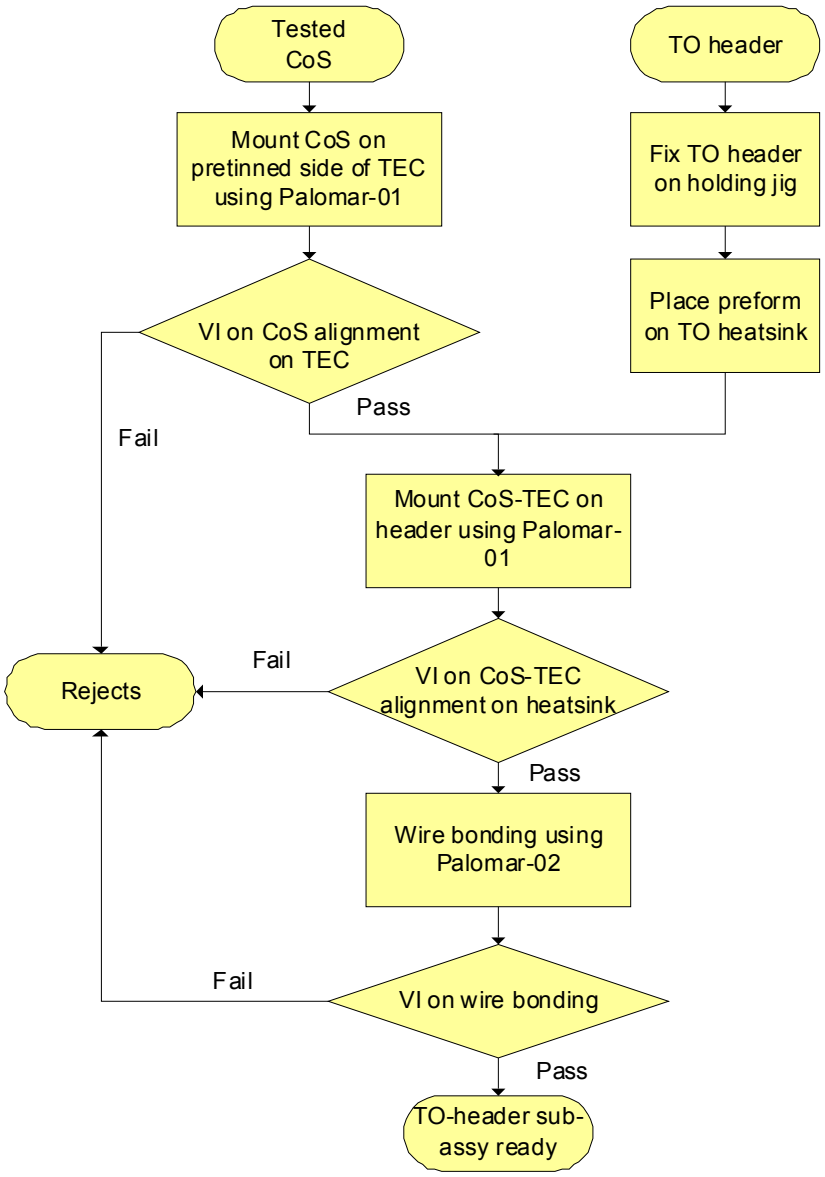


Figure 3-3: TO-header sub-assembly process flow

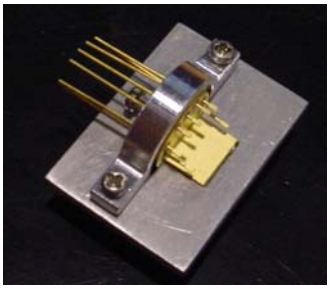
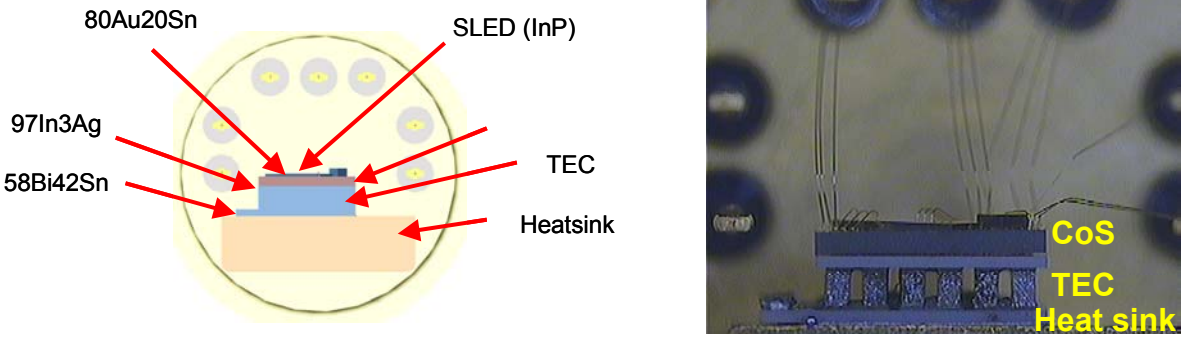


Figure 3-4: Holding jig for integration of CoS-TEC to heatsink on header

3.2.2.2 The solder scheme used in the integration of COS-TEC-header has to be carefully selected in consideration of the maximum temperature rating of the COS and TEC. The solder used should have a maximum temperature smaller than maximum rating of 220 °C of the TEC and higher than the storage temperature requirement of 85 °C. The temperature range within 130 to 200 °C is selected. In addition, the solder also need to have a thermal expansion coefficient that is close to the heatsink and SLED chip to avoid exerting undue stress on the chip. Table 3-1 shows the properties of the solder used in the integration process. The solders selected for the interface between different parts are shown in the schematic diagram of Figure 3-5.

Table 3-1: Property of solders selected

Part	Material	Melting temp. (degC)	CTE ($x10^{-6}$/degC)
Solder	80Au20Sn	280	16
Solder	97In3Ag	146	22
Solder	58Bi42Sn	138	14
SLED	InP	-	4.5
Submount	AlN	-	4.5
TEC	Ceramic	-	6.7
Heatsink	OFHC	-	9.4



(a) (b)

Figure 3-5: (a) Solder selected for integration of CoS-TEC-heatsink on header, (b) Assembly cross section of COS-TEC-heatsink with wire bondings

3.2.2.3 In order to check the strength of the bonding between the various interfaces, mechanical stress test is performed on the sub-assembly header:

i) Die shear: Between SLED chip and submount
ii) Ball shear: Between wire ball and submount
iii) Wire pull: Between bonding wire and the header lead
iv) COS shear: Between COS and TEC
v) TEC shear: Between TEC and heatsink of header

3.2.2.4 The mechanical stress performance between the layers indicated from i) to v) is tabulated in Table 3-2. Their measured performance are well within requirement, except for the low CoS shear force between the COS and TEC. This is due to application of solder preform on the top surface of TEC, which does not have the required adhesion strength to the TEC surface. A TEC with pretinned solder on its top surface will be used to increase this bonding force. However, due to the delay in delivery of the TEC with pretinned solder, this COS shear test is not repeated. The TEC unit is later changed to CuW block as the thermal interface between the COS and heatsink of the TO-header.

Table 3-2: Mechanical stress test

DIE SHEAR (>1570 g)	BALL SHEAR (>20 g)	WIRE PULL (>3 g)	COS SHEAR (>2500 g)	TEC SHEAR (>2500g)
5033g (Die crack first)	37.9g	10.7g	2088g	4511g
5111g (Die crack first)	38.2g	10.1g	2133g	5083g (TEC crack first)
4817g	41.1g	9.8g	2090g	5900g (TEC crack first)

3.2.2.5 Figure 3-6a illustrates the cracked die after going through the die shear test from the submount. Bonding between the die and submount is so strong that the SLED chip cracked with the solder still attached to the submount. Figure 3.6b shows the top

surface of TEC after COS shear. As solder perform is used, the bonding force is not strong enough and the solder is sheared off

(a) (b)

Figure 3-6: (a) Die shear from CoS, and (b) CoS sheared from TEC

3.2.2.6 Figure 3-7 shows the fully integrated COS-TEC-Header with wire bonding to the specified leads. The SLED chip used in the process development is selected from DS01 chip. The L-I curve of the SLED chip mounted on the TO-header is shown in Figure 3-8. Thermal roll-over at 80mW output at ~600 mA is due to over-temperature of TEC under CW operation of SLED.

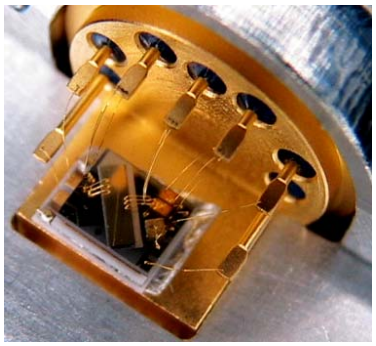


Figure 3-7: Integrated CoS-TEC-header with wire bonding

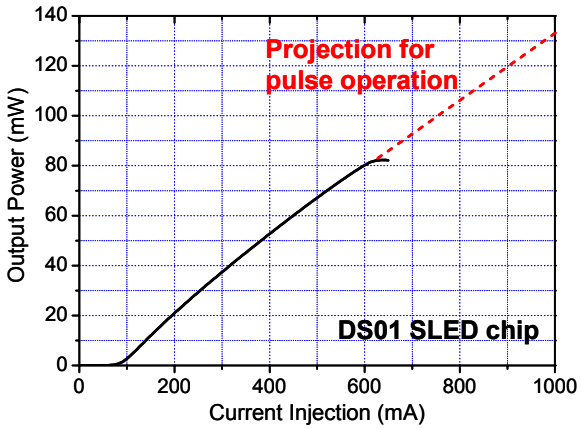


Figure 3-8: CW L-I curve of integrated CoS-TEC-header

3.3 TO-Header Capping Development (DP02)

3.3.1 *Design*

3.3.1.1 The TO canning process is completed with the provision of a hermetically sealed inert environment for the SLED chip on TO-header through welding of a TO cap to the TO header, as illustrated in Fig. 3-9.

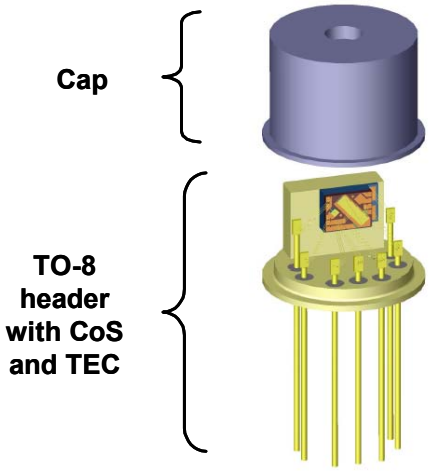


Figure 3-9: Designed TO-8 header with cap

3.3.1.2 The TO cap used in this project has a flat quartz window to allow the optical light to emerge from the TO can. Here, the diameter of the flat window and the cap height are carefully determined so that the diverging light from the SLED chip is not blocked by the metal part of the cap. In addition, the quartz window is also anti-reflection coated to minimize reflection back into the SLED chip, which would be detrimental to its operation.

3.3.2 *Process Development and Results*

3.3.2.1 Figure 3-10 shows the developed process flow of TO-header capping. The capping process comprises firstly outgassing of the component to obtain low moisture and oxygen content before electrical welding of the cap to achieve hermetic sealing. Leak test and temperature cycling are carried out to check that this process fulfills the required criteria.

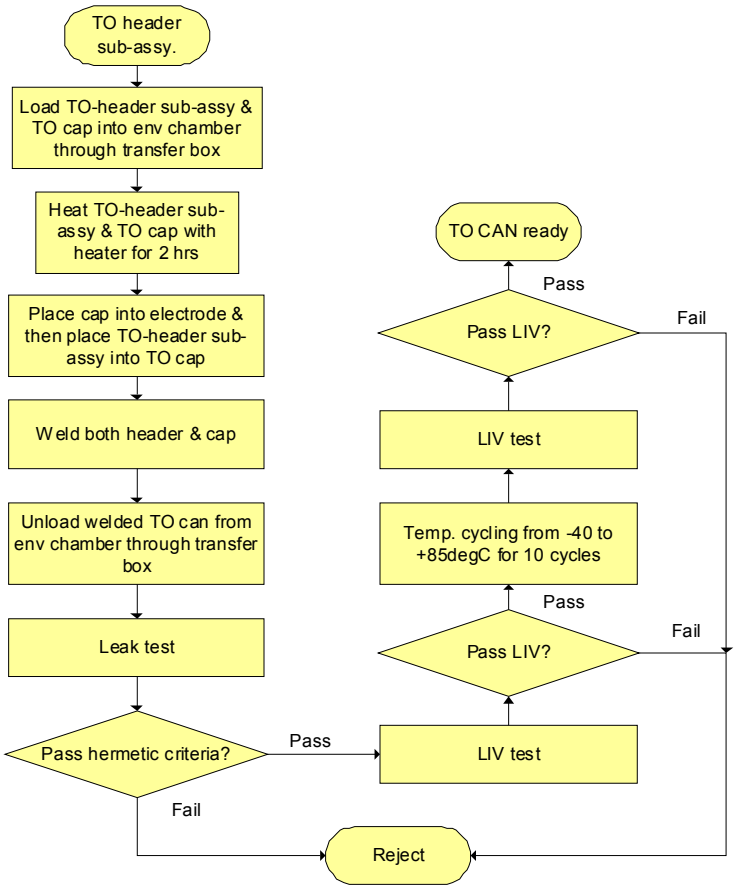
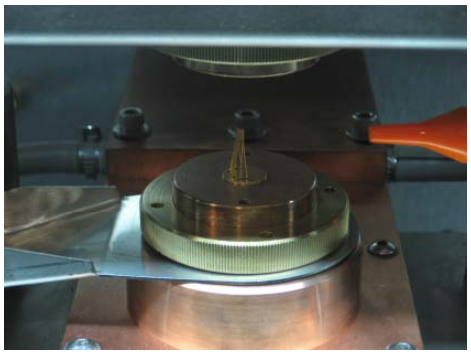


Figure 3-10: Developed TO capping process flow

3.3.2.2 Electrical welding is carried out by first placing the TO can into the electrode and then the TO-header sub-assembly into the TO cap. The welding electrode is designed with an accuracy of +/-0.001" ~ 0.002" (+/-0.025 to 0.05 mm) in holding the parts together during the process. Figure 3-11 illustrates the projection welder chamber and TO-header sub-assembly in the electrode during the capping process.

(a)



(b)

Figure 3-11: (a) Projection welder in environment chamber and
(b) TO header sub-assembly loaded into TO cap in electrode

3.3.2.3 In order to check quality of the capping process, leak test, residual gas analysis and temperature cycling have been performed. In the leak test, 10 units TO cans have been bombarded with helium at 60PSI for two hours. A leak rate of $<10^{-8}$ cc/sec has been detected, demonstrating that the process is well controlled as per Telcordia requirement.

3.3.2.4 Residual gas analysis has also been carried out to check the gas content in the TO can. The test was performed with reference to ORS SOP MEL-1053 based on Commercial Practice for Internal Vapor Analysis and the test outcome meets Telcordia requirement of <5000 ppm of moisture. Table 3.3 shows the residual gas content in the TO can after the capping process. The oxygen and moisture levels are within the requirement.

Table 3-3: Test report of interval vapor analysis of capped TO cans

Sample ID	1	2	3	Unit
Pressure	94.6	94	93.6	Torr
Nitrogen	99.6	99.6	99.5	%
Oxygen	2170	2049	2345	ppm
Argon	184	171	184	ppm
CO2	<100	<100	<100	ppm
Moisture	742	978	1897	ppm
Hydrogen	489	272	602	ppm
Helium	ND	ND	ND	ppm
Fluoro-Carbons	ND	ND	ND	ppm
Unknown*	ND	194	ND	ppm

Note:

Unknown* : NIST database best identified unknown as Styrene, C8H8
ND : None detected
1% : 10,000ppm
Pressure : Inlet chamber pressure

3.3.2.5 In addition, the completed TO-cap units were subjected to temperature cycling for 10 cycles from –40 to +85 °C. The change of optical power is measured to be <+/-5% after the temperature cycling process, as shown in Figure 3-12.

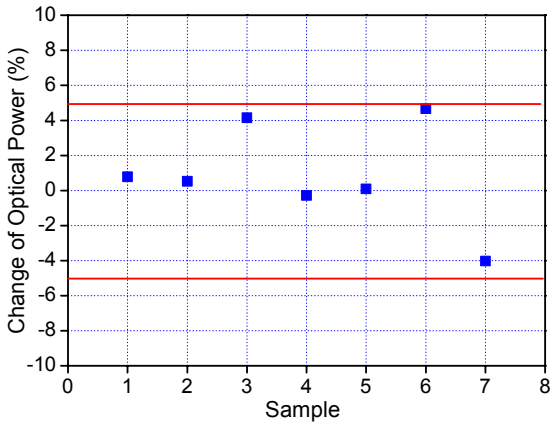


Figure 3-12: Power change after 10 cycles of temperature cycling from -40 to +85 °C for TO capped unit

3.3.2.6 Besides the above tests, assessment of the mechanical strength between the TO-header and cap is also carried out by applying a clamping force to the TO can. Figure 3-13 shows the TO can before and after the clamping test. It can be seen that the material of TO cap is torn off while the welding joint is still intact. This proves that mechanical strength of the welding joint is stronger than that of the material of the TO cap (50 Ni-Fe).

(a) (b)

Figure 3-13: TO-cap (a) Before clamping test, and (b) After clamping test

3.3.2.7 The L-I curve of the SLED in the TO capped unit is shown in Figure 3-14. It is noted that the measured curve matches very closely to that of the SLED CoS, demonstrating that almost all the light emitted by the SLED chip emerges from the TO can and there is minimal light blockage by the cap. The roll-over at 80 mW output is due to over-temperature of TEC under CW operation of SLED.

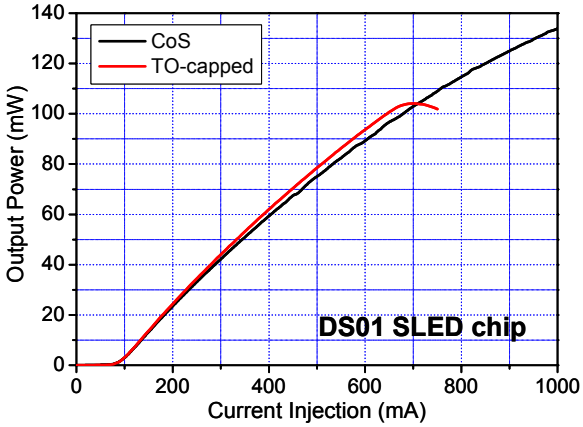


Figure 3-14: L-I test result of TO-8 capped unit, compared to that at CoS level

3.4 TOSA Assembly Development (DP03)

3.4.1 *Design*

3.4.1.1 The diverging SLED light output from the packaged TO can is to be collimated with an aspherical lens to realize low beam divergence, forming a Transmitter Optical Sub-Assembly (TOSA).

3.4.1.2 A number of design considerations have to be looked into in order to realize low 2 mrad divergence collimation. One of the key considerations is the design specifications for collimating lens (asphere, EFL, aperture, etc) and its assembly technique. Different lens from Alps, Anteryon, LightPath Tech and Jena have been studied for current TOSA implementation.

3.4.1.3 For the TOSA assembly process, typical +/-10 µm order of magnitude tolerances of assembly parts and processes cannot support passive alignment to meet the project target requirement (not even for 10 mrad). Active alignment assembly process development is necessary, with DP03 (10 mrad) as first milestone to be achieved before progression to DP04 (2 mrad).

3.4.1.4 The following variations are considered in the design of the optical lens and assembly process for the TOSA:

a) Tolerances of dimensions of all mechanical parts and optics
b) Tolerances of SLED chip far-field optical mode (due to wafer fabrication process tolerances)
c) Tolerances of sub-assemblies (e.g. placement of chip with respect to the header datum)
d) Tolerances of optics and their mounting alignment
e) Tolerances of active alignment of TOSA (6-axis sub-micron precision tool to be employed) and maintenance of alignment precision during TOSA assembly process

f) Operating ambient/case temperature variations (impairment to optical alignment)
g) Operational vibrations/shock (design-in reliability concept)

3.4.1.5 Figure 3-15 shows the simulation results of divergence angle with reference to z-axis offset for lenses of different focal lengths. By increasing the focal length, the divergence angle is less sensitive to the z-axis offset. In DP03, an Alps lens FLAN1Z101 with focal length of 1.81 mm and numerical aperture (NA) of 0.3 has been selected to realize <10 mrad of divergence. The proposed mounting of the lens on the cap is depicted in Figure 3-16. The simulated distribution of axial z offset of the lens is shown in Figure 3.17a with the tolerance of each component tabulated in Figure 3.17b.

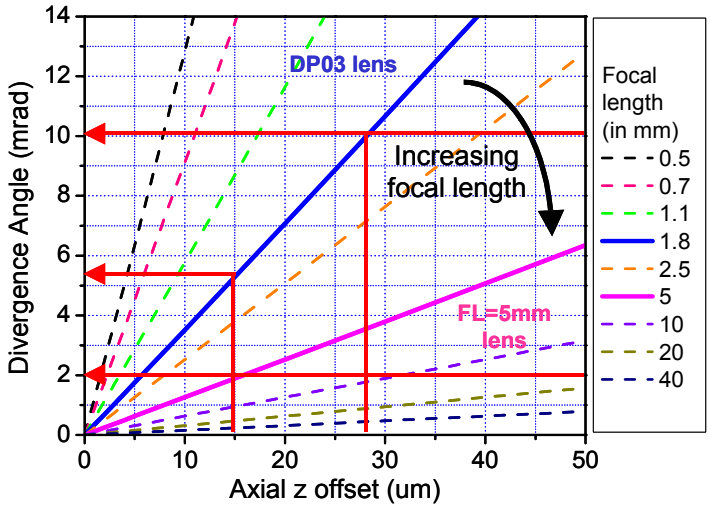


Figure 3-15: Simulation of divergence angle versus axial z offset for lenses of different focal lengths

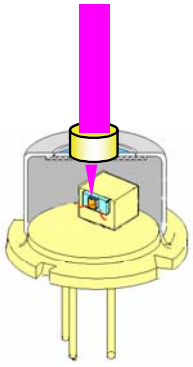
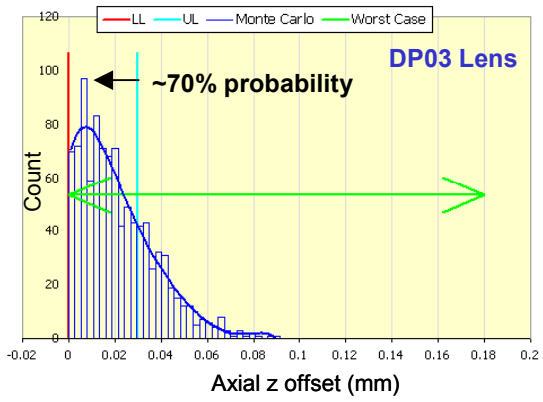


Figure 3-16: DP03 Alps aspherical lens with active alignment and mounted directly on TO-window cap.



(a)

Axial tolerance (μm)	
Lens WD	+/-0.03
Cap height	+/-0.03
TO-based height	+/-0.05
Heatsink block	+/-0.03; -0.05
CoS-TEC-header assy	+/-0.02
Lens assembly	+0.02; -0

(b)

Figure 3-17: (a) Simulated distribution of axial z offset outcome of DP03 lens using Monte Carlo Analysis, and (b) Axial tolerance used in simulation

3.4.2 *Process Development and Results*

3.4.2.1 The assembly and integration of the DP03 lens with the TO-8 can is performed using a 6 axis translation stage, as illustrated in Fig. 3-18. The beam divergence is monitored live during assembly with a Goniometric radiometer. A typical beam divergence plot of SLED on TO-header sub-assembly with DP03 lens from Alps is shown in Figure 3-19. A divergence angle of ~10 mrad has been achieved.

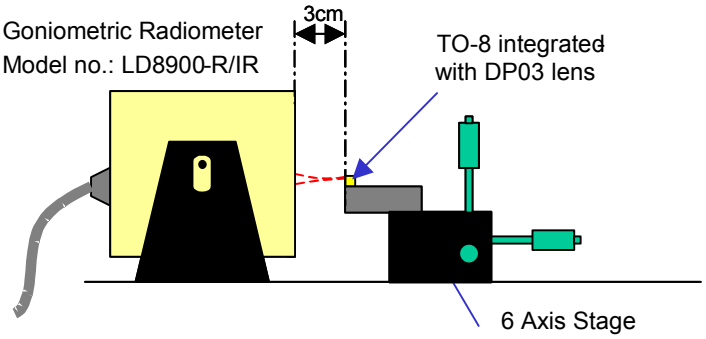


Figure 3.18: Beam divergence setup using Photon Inc Goniometric Radiometer

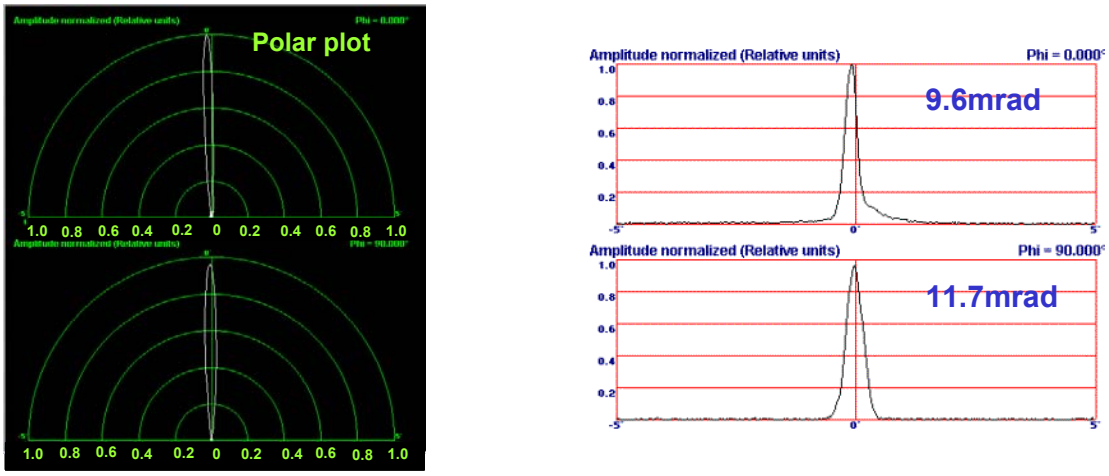


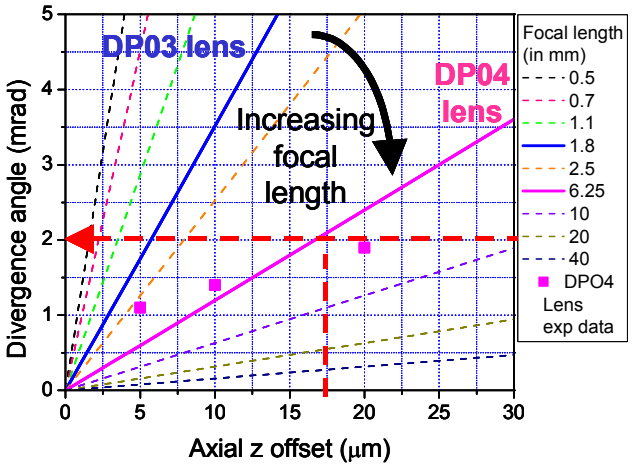
Figure 3-19: Beam divergence of SLED on TO-header sub-assembly after collimation with DP03 lens (measured with Goniometric Radiometer)

3.4 TOSA Assembly Optimization (DP04)

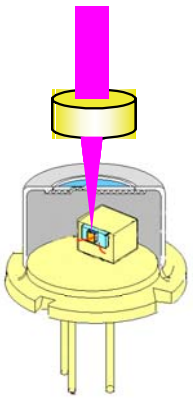
3.4.1 *Design*

3.4.1.1 To improve the collimation of 10 mrad in DP03 to the target value of <2 mrad in DP04, an aspherial lens of larger focal length has to be used. From the simulation results in Fig. 3-20a, it is clear that a lens with focal length of >6 mm is required to achieve a divergence angle of <2 mrad.

3.4.1.2 In DP04, an Anteryon lens AC355 with focal length of 6.25 mm and numerical aperture (NA) of 0.3 has been selected to achieve <2 mrad of divergence angle. The proposed scheme of mounting of the lens on the cap is depicted in Fig. 3-20b. The simulated distribution of axial z offset of the lens is shown in Figure 3-21.



(a)



(b)

Figure 3-20: (a) Simulation of divergence angle versus axial z offset for different focal lengths, (b) DP04 Anteryon lens with active alignment and mounted at a distance from the cap

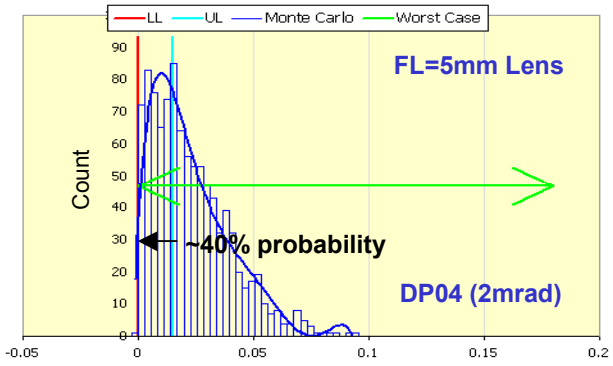


Figure 3-21: Simulated distribution of axial z offset of DP04 lens using Monte Carlo Analysis

3.4.2 *Process Development and Results*

3.4.2.1 The setup of the assembly of the TOSA module is illustrated in Figure 3-22. The TOSA is mounted on a 6-axis translation stage, and active alignment is performed by projecting the light from the TOSA through mirrors to the beam scan detector located at 1.75 m away from the light source. The lens is affixed onto the TO can with epoxy once the target beam profile is achieved. A completed TOSA module is shown in Fig. 3-23.

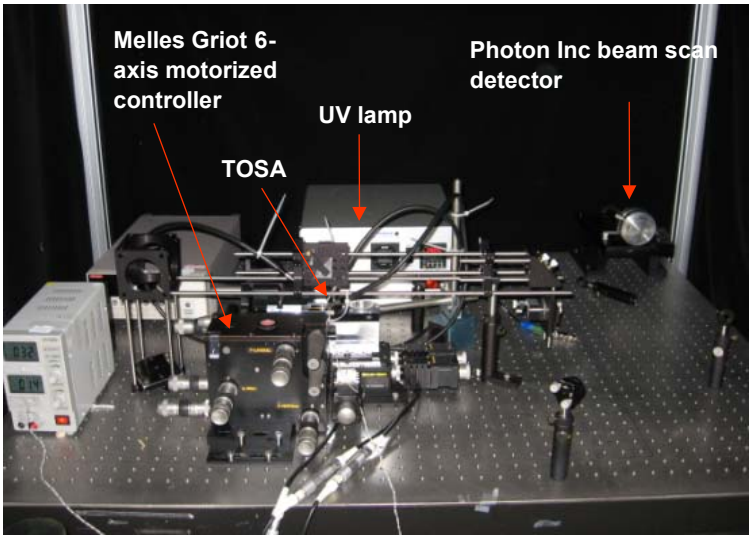


Figure 3-22: TOSA assembly stage with epoxy UV curing lamp

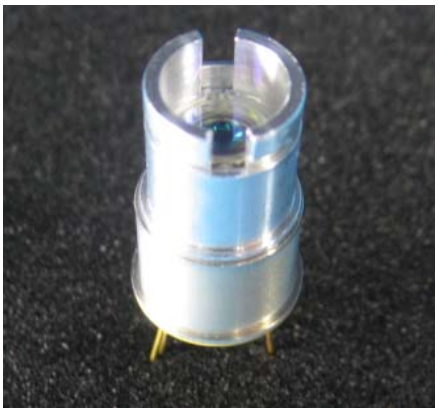
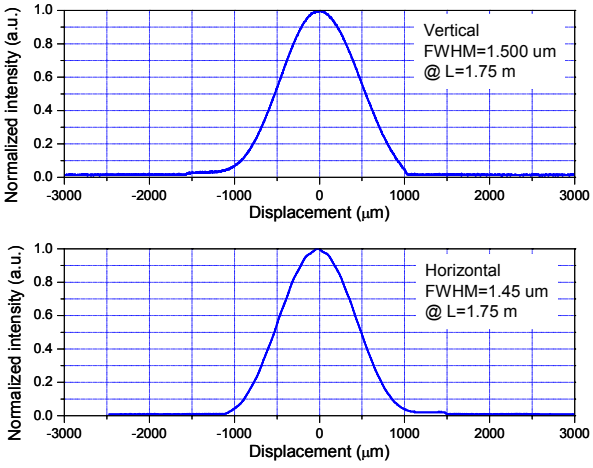


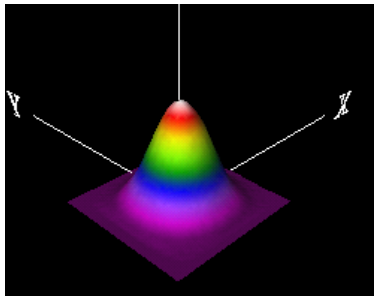
Figure 3-23: Completed TOSA with DP04 lens

3.4.2.2 Figure 3-24 shows the optical far-field mode profile of the SLED TOSA measured by the beam scan detector. A beam divergence of around 1 mrad has been achieved, as also confirmed by the following computations:

Distance between SLED & detector, L = 1.75m
Measured beam diameter at L, D = 1.5mm
SLED TOSA FOV $= 2 \cdot \tan^{-1}(D/(2L))$
$= 2 \cdot \tan^{-1}(1.5 \times 10^{-3}/(2 \times 1.75))$
$= 0.9$mrad



(a)



(b)

Figure 3-24: TOSA mode profile (measured by beam scan detector)
(a) Plot of far-field CW: I_F = 350 mA, and (b) 3D far-field plot of divergence

3.4.2.3 The electrical and optical characteristics of the TOSA have been evaluated. Figure 3-25a and b shows the CW optical power versus forward current and forward voltage versus forward current respectively. CW optical power output of 40 mW at operating current of 350 mA is achieved.

3.4.2.4 The TOSA peak power test is carried out with pulse width of 2 µs, duty ratio of 0.1% and Keithley pulsed electronics driver, and the measured result is shown in Figure 3-25c. A TOSA optical peak power of 160 mW has been achieved. When compared to the TO can emission power, there is an excess optical loss of ~25% after TOSA assembly. This is likely due to some blockage of light by the collimating lens mount to the TO-8 can.

3.4.2.5 Figure 3.26 shows the optical spectrum of the SLED TOSA obtained from an optical spectrum analyzer. The measured center wavelength of the broadband emission is ~1550 nm.

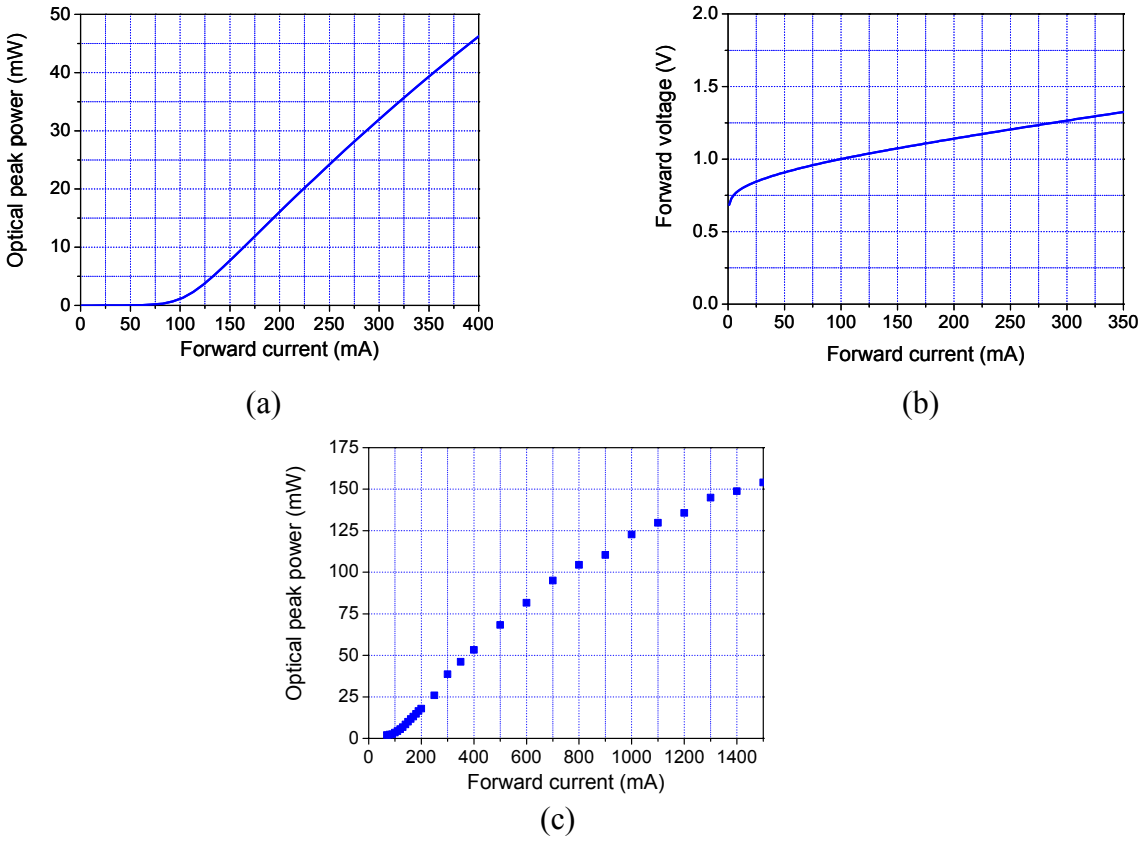


Figure 3.25: (a) CW power vs. forward current, (b) Forward voltage vs. forward current, and (c) Pulsed peak power vs. forward current with pulse width of 10ns, duty ratio of 0.1%

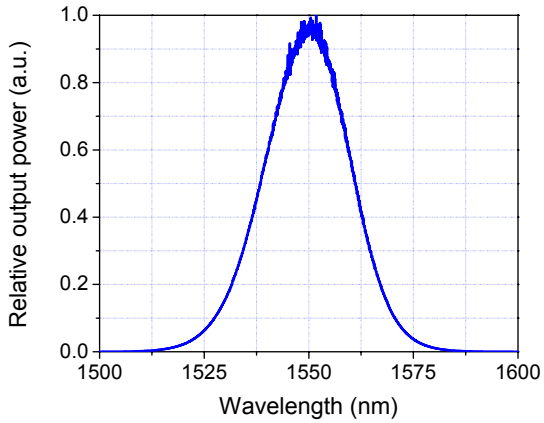


Figure 3.26: Optical spectrum of SLED TOSA

3.5 Summary

3.5.1 The SLED chip has been successfully packaged into a compact 7-pin TO-8 platform TOSA with built-in collimating aspherical lens. Good matching of collimation optics with SLED optical mode profile, together with packaging mechanical design and assembly process optimization, has enabled the achievement of a very low beam divergence of 1mrad.

4. Device Test Development

4.1 Organization of Design Stages

4.1.1 The SLED device test development involves design of divergence test methodology and test setup, and design of electronic circuit to drive the TOSA for fast pulse testing with high drive current. It is organized into the following stages:

DTO01 (TOSA test development):

In this first stage, the test methodology for beam divergence measurement will be established, together with building up a test setup for beam divergence measurement capability down to <10 mrad.

DTO02 (TOSA test refinement):

Subsequently, improvement on the beam divergence test setup will be performed to enable measurement down to <2 mrad.

DTH01 (Pulse test development):

Here, the electronic pulse drive test circuit is designed and fabricated to match with the SLED electrical characteristics. A fast pulse measurement test setup is to be built up with rise and fall times measurement capability of <5 ns.

DTH02 (Pulse test refinement):

Refinement on electronic pulse test circuit design is carried out to allow for direct mounting of the SLED TOSA onto test evaluation board so as to realize rise and fall times of <1 ns.

4.2 TOSA Test Development (DTO01)

4.2.1 Figure 4-1 shows the beam divergence test platform set up based on the goniometric radiometer. The TO-header sub-assembly integrated with DP03 lens (short focal length) is mounted onto a 6-axis translation stage to align its output beam into the goniometric radiometer detector. The divergence angle can be obtained directly through the measured 2-D plot. The measurable beam divergence is around 10 mrad, as shown in Fig. 4-2

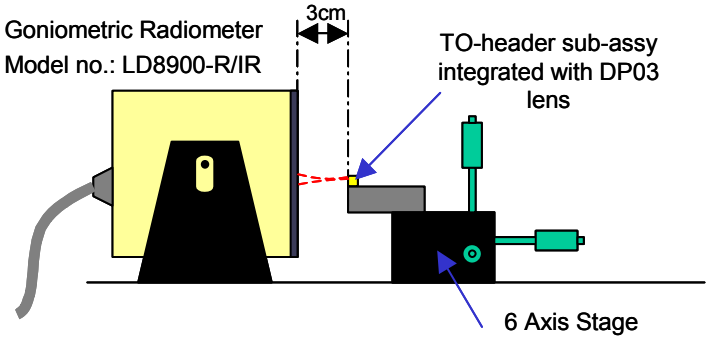


Figure 4-1: Beam divergence setup using Photon Inc Goniometric Radiometer

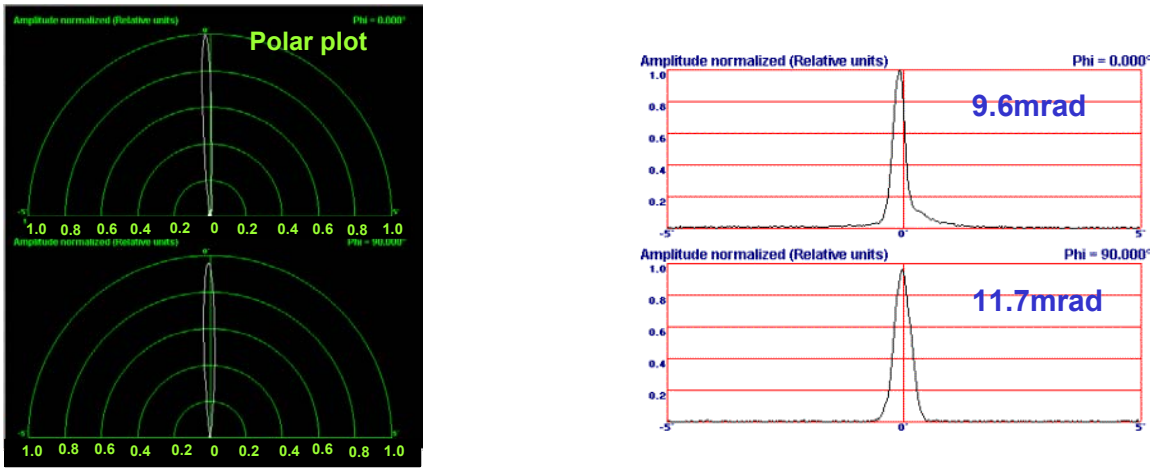
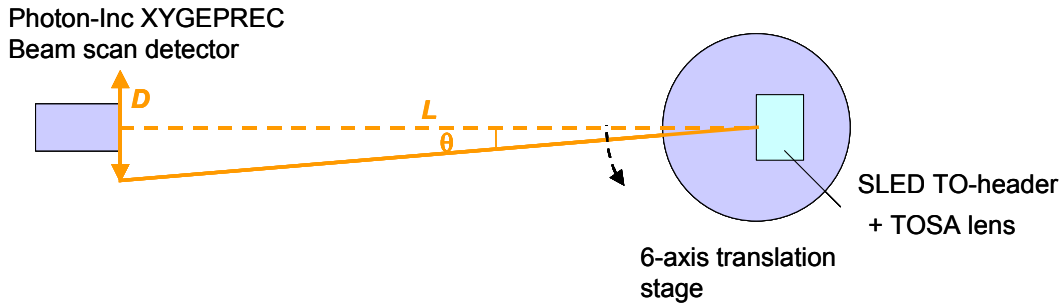


Figure 4-2: Beam divergence of SLED on TO-header sub-assembly
after collimation with DP03 lens

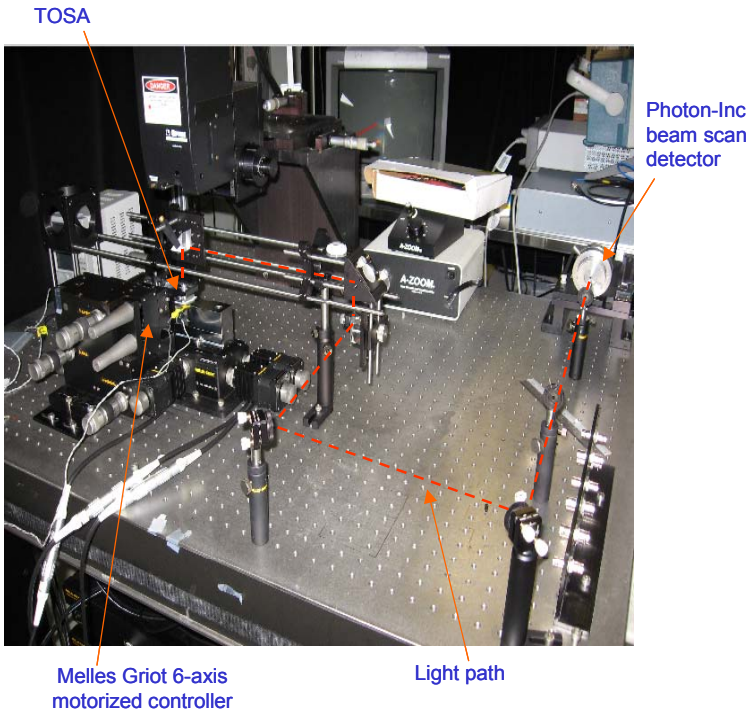
4.3 TOSA Test Refinement (DTO02)

4.3.1 In order to measure the optical beam divergence down to sub-mrad resolution, a Photon-Inc. beam scan detector is used to characterize the SLED TOSA light emission at a distance L from the emitter (Fig. 4-3a and b). The 2-D and 3D mode profiles of the TOSA are generated by the instrumentation, and the optical beam divergence subsequently determined as follows:

Distance between SLED TOSA and detector, L = 1.75m
Measured beam diameter at L, D = 1.4mm
SLED TOSA FOV $= 2 \cdot \tan^{-1}(D/(2L))$
$= 2 \cdot \tan^{-1}(1.46 \times 10^{-3}/(2 \times 1.75))$
$= 0.8$mrad



(a)

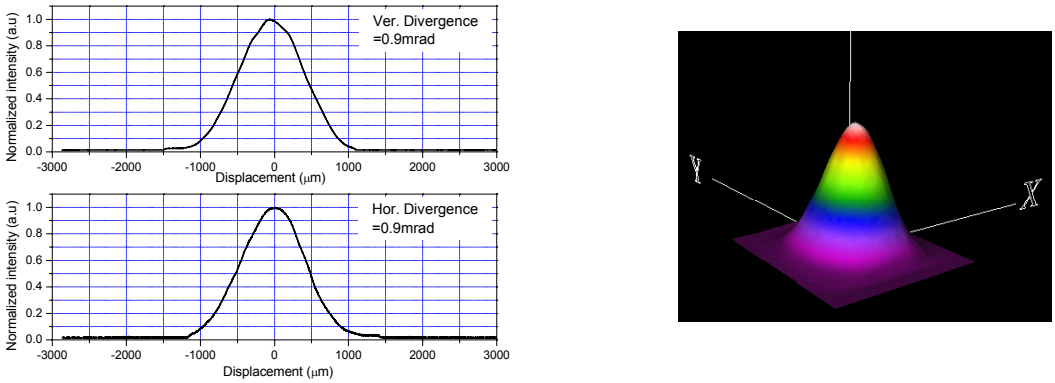


(b)

Figure 4-3: (a) Schematic diagram and (b) experimental setup for sub-mrad resolution beam divergence measurement

4.3.2 Figure 4-4 shows the optical mode profile of the SLED TOSA measured by the beam scan detector in the setup of Fig. 4-3. The variation of measured FWHM with scan detector displacement is plotted in Fig. 4-5. The field of view (FOV) is also independently determined from the gradient of the fitted line:

Gradient of fitted line = 2·tan(FOV/2)
For horizontal FF,
Gradient = 0.08/130 = 6.2×10^{-4}
FOV = 0.6mrad
For vertical FF,
Gradient = 0.15/130 = 1.15×10^{-3}
FOV = 1.1mrad



(a) (b)

Figure 4-4: TOSA mode profile measured by beam scan detector
(a) plot of far-field CW: I_F=350 mA, and (b) 3D far-field plot of beam profile

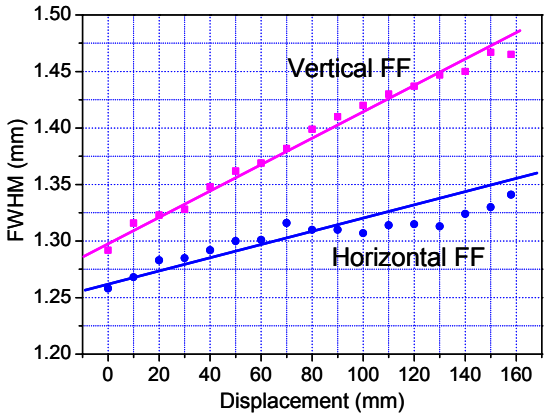


Figure 4-5: Variation of SLED TOSA beam FWHM with scan detector displacement

4.3.3 From the above described measurement setup and computation methodology, it has been demonstrated that the optical beam divergence test setup is capable to characterizing the beam divergence down to at least 1 mrad.

4.4 Pulse Test Development (DTH01)

4.4.1 The Directed Energy Inc. IXLD02 pulse driver is first used to drive the SLED TO-8 platform for pulse test characterization. The IXLD02 IC is an ultra high-speed differential laser diode driver capable of drive current upto 2 A. In addition, its maximum operating frequency of 17 MHz, pulse width of <1.5 ns and pulse rise and fall times of 600 ps meets the requirements of the pulse test setup. Figure 4-6 shows the schematic test setup based on the Directed Energy IXLD02 IC.

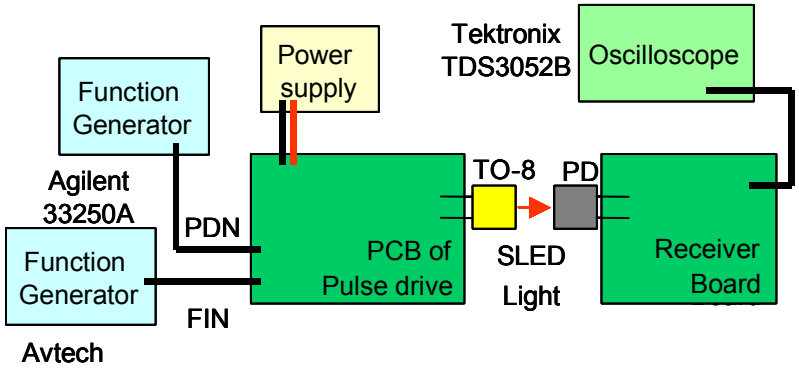
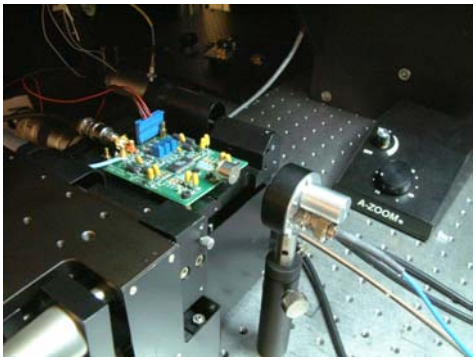
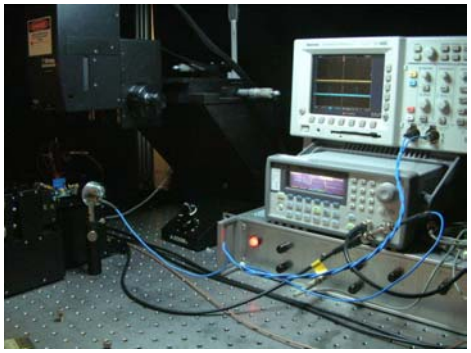


Figure 4-6: Schematic of pulse test setup of SLED TO-8



(a)



(b)

Figure 4-7: (a) TO can mounted on pulse drive board and facing PD,
(b) Measurement equipment for pulse test characterization

4.4.2 Figure 4-7 illustrates the TO can mounted on the pulse driver board and equipment setup for the pulse test characterization. Output light from the SLED is collected into the PD, and the received electrical signal is analyzed using the Tektronix pulse test equipment. Details of the test setup are explained in section 4.5.

4.4.3 Different types of PIN PD have been selected to characterize the fast rise and fall times of the received signal so that the optical pulse signal could be captured accurately. Table 4-1 tabulated the specifications from 1) New Focus 1414, 2) Mitsubishi GNOK-PD708C8 and 3) Perkin Elmer C30618 PDs. The signal detected from each PD is

shown in Figure 4-8. The New Focus PD is able to capture modulation rise time of <1 ns and hence is selected for the SLED TOSA pulse test characterization.

Table 4-1: Different PDs used to characterize rise and fall times of received signals

PD model	New Focus 1414	Mitsubishi GNOK-PD708C8	Perkin Elmer C30618
PD Diameter	25 um	80um	300um
PD 3dB BW	25GHz	3GHz	0.75GHz
PD rise time	<0.02ns	<1ns	<1ns
PD dark current	N/A	<2nA	<5nA
Responsivity	0.6A/W	0.8A/W	0.7A/W
Modulation rise time	~0.6ns	~1.5ns	~2.3ns
Modulation fall time	~0.9ns	~1.7ns	~2.3ns

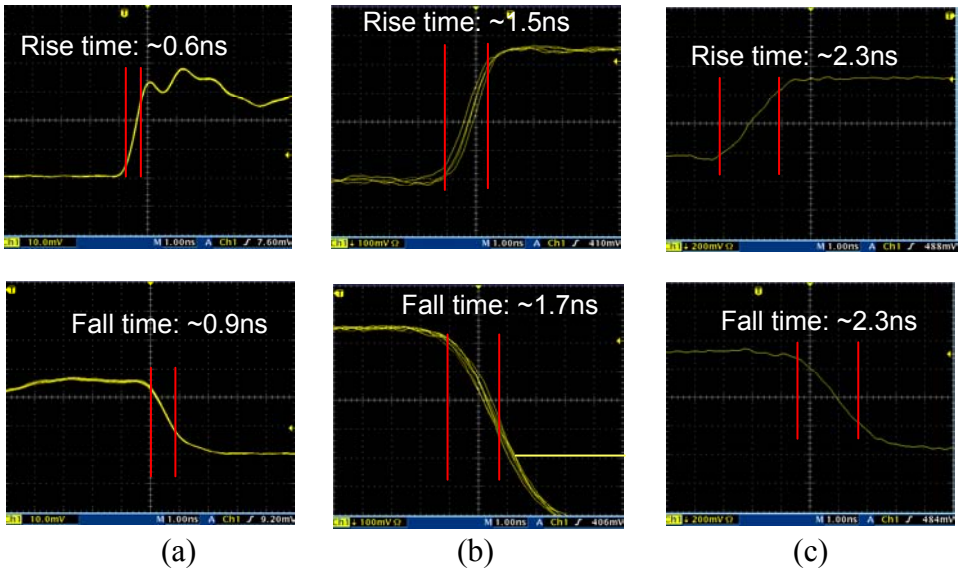


Figure 4-8: SLED light received using (a) New Focus 1414 PD, (b) Mitsubishi PD708C PD, (c) Perkin Elmer C30618 PD

4.4.4 Figure 4-9 shows the test setup for average optical power measurement using a calibrated integrating sphere 2500INT-2-IGAC and Keithley Model 2500 Dual Photodiode Meter. The computed peak power from the measured average optical power, pulse width and repetition rate is shown in Figure 4-10, whereby the measured average optical power scales linearly with the pulse width and repetition rate. A peak optical power of close to 220 mW at ~1.5 A pulsed current drive is achieved using DS02 SLED chip.

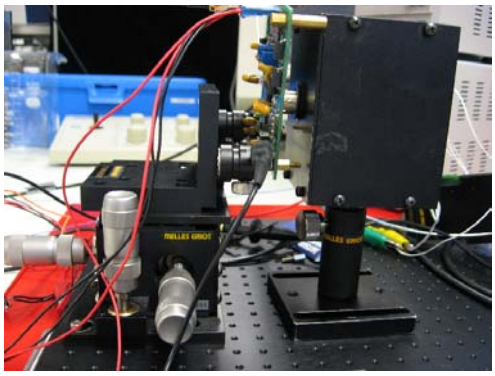
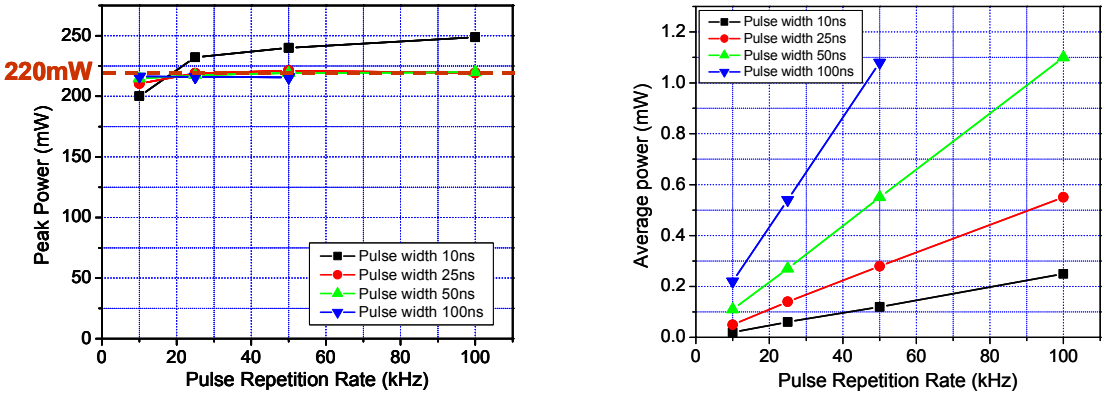


Figure 4-9: Integrating sphere 2500INT-2-IGAC and Keithley Model 2500 Dual Photodiode Meter for average power measurement



(a) (b)

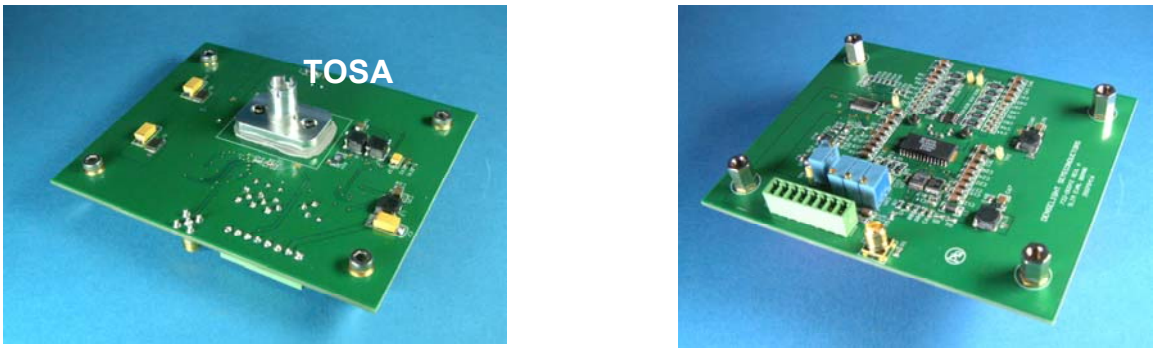
Figure 4-10: (a) Computed peak power vs pulse repetition rate,
(b) Measured average power vs pulse repetition rate

4.5 Pulse Test Refinement (DTH02)

4.5.1 In order to improve the test functionality and mounting of SLED TOSA, an evaluation board (Eval-board) is designed and fabricated based on the key features of the IXLD02 board used in DTH01.

4.5.2 The Eval-board is complete with mounting for the SLED TOSA and essential drive electronics to support a comprehensive range of testing with minimal external electronics instrumentation. Figure 4-11 shows an example of how the SLED can be clamped onto the evaluation board for thermal dissipation, together with short leads for low-inductance high-speed (<1 ns rise/ time) pulse drive of the SLED light output over various ranges of power level, pulse width and pulse repetition rate. A temperature controller is also included in the Eval-board to operate the internal TEC (if available) of the SLED TOSA and thereby setting the chip temperature of the SLED device

.



(a) (b)

Figure 4-11: a) Bottom side, and b) Top side of Eval board

4.5.3 The mechanical layout of the Eval-board is shown in Figure 4-12a and b. Key features of the Eval-board include:

i) Use simple lab power supplies (+5 V, +7 V)
ii) Mounting clamp for SLED TOSA unit
iii) Preset for 0 to 2 A variable pulse current
iv) Preset for 10 ns to 300 ns pulse width
v) User defined pulse repetition rate/pattern via external trigger input (CMOS/TTL-logic)
vi) Preset chip operating temperature from 0 to 40 °C

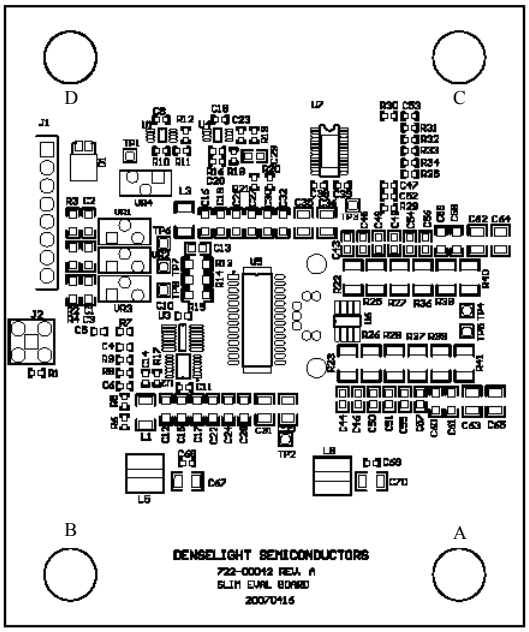


Figure 4-12a: Top-side mechanical layout of evaluation board

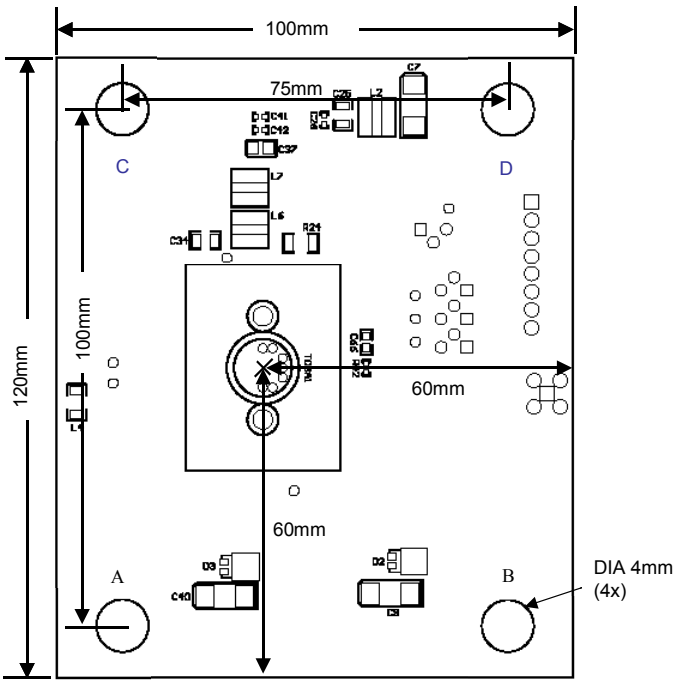


Figure 4-12b: Bottom-side mechanical layout of evaluation board

4.5.4 Table 4-2 shows the pin assignment and functions of connectors of the Eval-board. The 8-pin header provides power supply to the TEC and LD driver. The external trigger input is via SMA connector (J2). All monitoring signals for various component functions, for example, TEC temperature or LD anode and cathode voltages, can be accessed through test point connectors TP1 to TP8.

4.5.5 The received electrical signal from the pulsed SLED TOSA is measured by guiding the collimated light output from the SLED into the New Focus 1414 high-speed photodetector using a fiber connector and monitoring the output with an oscilloscope through matched high-speed cable, as shown in Fig 4-13. A typical trace of pulse is shown in Fig. 4-14 with the following key parameters:

i) Rise time and fall time of <1 ns.
ii) Pulse width = 10 ns
iii) Pulse repetition rate = 100 kHz

Table 4-2: Pin assignment and function of evaluation board

Label	Connector Type	Pin No.	Description
J1	8-pin Header	1	Power supply ground
		2	+5V D.C.
		3	Power supply ground
		4	+5V D.C.
		5	Power supply ground
		6	+7V D.C.
		7	NC
		8	NC
J2	SMA		External Trigger Input (CMOS/TTL compatible)
TP1	Test Point Connector		To monitor TEC temperature
TP2	Test Point Connector		GND
TP3	Test Point Connector		GND
TP4	Test Point Connector		To monitor light source Anode voltage
TP5	Test Point Connector		To monitor light source Cathode voltage
TP6	Test Point Connector		To monitor voltage across VR1 that control current IIBI, flowing into IBI pin of IXLD02 high-speed LD driver IC that is used as baseline current with respect to IIPW current to compensate for internal delays.
TP7	Test Point Connector		To monitor voltage across VR2 that control current IIOP, flowing into IOP pin of IXLD02 high-speed LD driver IC that is used to tune LD current
TP8	Test Point Connector		To monitor voltage across VR3 that control current IIPW, flowing into IPW pin of IXLD02 high-speed LD driver IC that is used to tune LD current pulse width

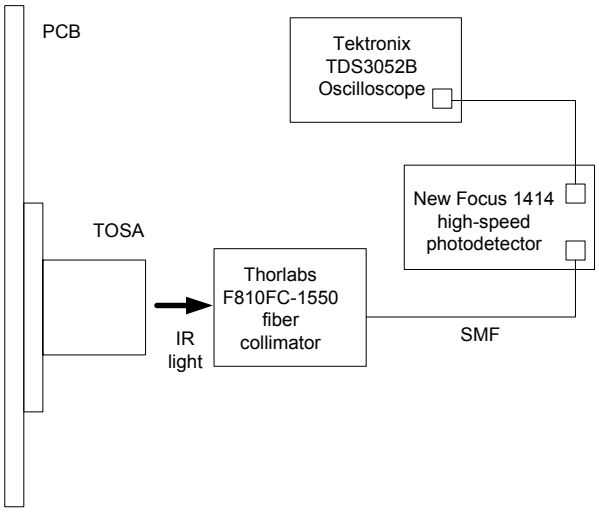
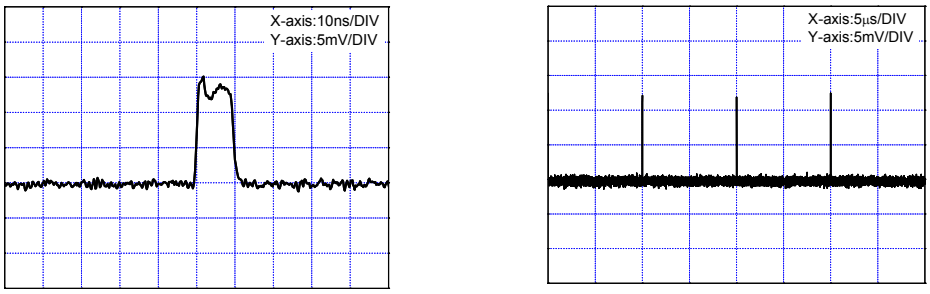


Figure 4-13: Pulsed optical signal measurement setup



(a) (b)

Figure 4-14: Scope trace of (a) Single pulse, and (b) Pulse train, with pulse width = 10 ns and repetition rate = 100 kHz

4.5.6 The pulse width of the SLED current drive can be tuned via variable resistors VR1 and VR3. VR1 controls the current I_{IBI}, flowing into IBI pin of IXLD02 high-speed LD driver IC that is used as a baseline current with respect to I_{IPW} current to compensate for internal delays. Resistor VR3 controls the current I_{IPW}, flowing into IPW pin of IXLD02 high-speed LD driver IC that is used to tune the SLED current pulse width. Turning the VR1 and VR3 in clockwise direction will reduce the I_{IBI} and I_{IPW}, while anti-clockwise rotation will increase both values. The voltage across VR1 and VR3 can be monitored via TP6 and TP8 respectively. The value of I_{IBI} should be higher than I_{IBI}. If I_{IPW}=I_{IBI}, the pulse width is 0. As I_{IPW} approaches I_{IBI} but less than I_{IBI}, the pulse width becomes smaller. Figure 4-15 illustrates the relationship of current pulse width t_{PW} versus I_{IPW} with respect to I_{IBI}.

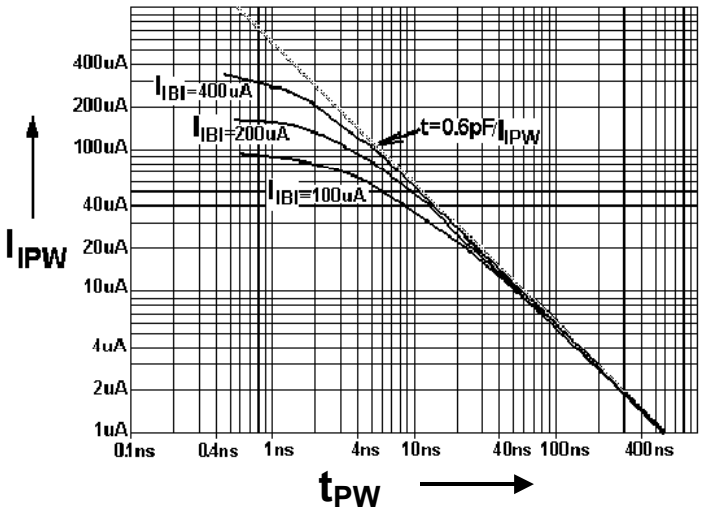


Figure 4-15: Current pulse width versus IPW current (Abstracted from page 5 of IXLD02 Ultra high-speed laser diode driver IC specification from Directed Energy Inc.)

4.5.7 The output current that drive the SLED can be tuned via variable resistor VR2 that controls current IIOP flowing into IOP pin of IXLD02 high-speed LD driver IC, and the voltage across VR2 can be monitored via TP7. The voltage across the SLED can be obtained from measurement of voltage difference between TP4 (TP3 as GND) and TP5 (TP2 as GND) using an oscilloscope.

4.5.8 The temperature of the TEC unit inside the TO-can, if available, can be tuned via variable resistor VR4. The voltage across VR4 is monitored via TP1. Figure 4-16 shows the corresponding TEC temperature with TP1 voltage. The maximum driving current and voltage of the TEC is set at 1 A and 2 V respectively, with nominal setting at 25 °C.

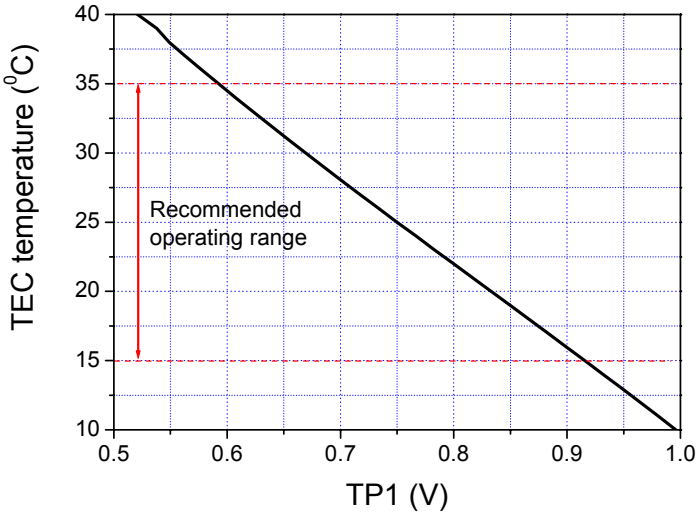


Figure 4-16: Dependence of TEC temperature with TP1 voltage

4.6 Summary

4.6.1 The measurement methodology and test setup for optical beam divergence of the SLED TOSA have been developed and refined to enable characterization down to at least 1 mrad resolution.

4.6.2 An evaluation board has also been developed with high speed and high current drive electronics to allow for improved test functionality and direct mounting of SLED TOSA onto the board. Fast rise and fall times of <1 ns of SLED drive pulses have been realized with the evaluation board.

5. Sample Unit Preparation and Test

5.1 Configuration of Sample Units

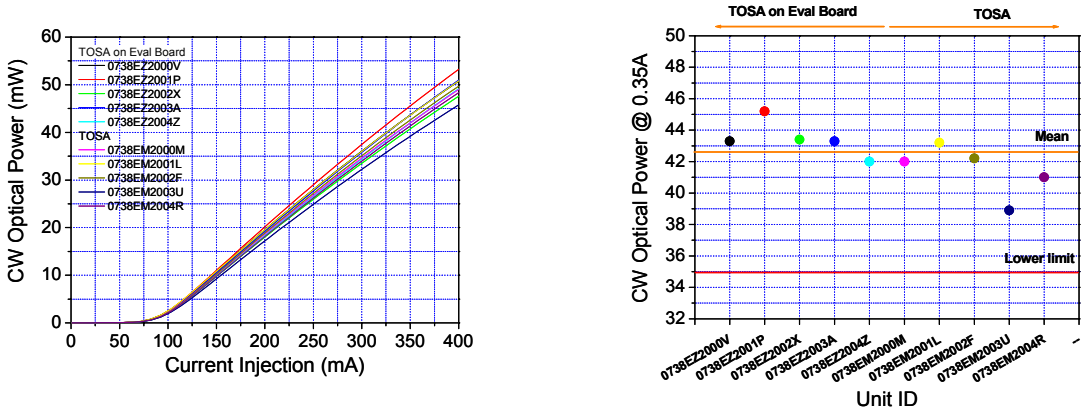
5.1.1 Ten units of SLED TOSA are prepared and packaged as samples. The SLED chip used is based on the DS03-A design (7QW structure of 2 mm length with doping optimization). As delivery of the selected microTEC unit from Marlow is very much delayed because of need for ITAR license grant, the TO-header sub-assembly is redesigned for uncooled operation, with the TEC unit replaced by a CuW block for heat dissipation.

5.1.2 Out of the ten SLED TOSA samples, five units are mounted onto DenseLight designed evaluation board for ease of test verification. All the ten samples have been fully tested and characterized.

5.2 Performance and Results

5.2.1 *CW Optical Power, Current Drive and Forward Voltage*

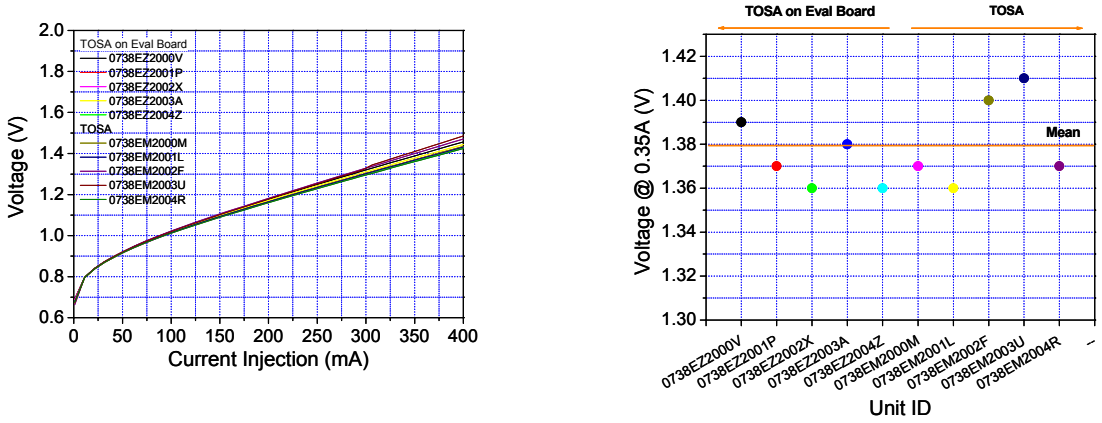
5.2.1.1 The TOSA samples are first characterized for their CW optical power versus current drive characteristics at 25 °C thermistor readout of SLED chip temperature (T_{SLED}). Figure 5-1 shows the measured CW optical power with forward current and distribution of the optical power at 0.35 A for the 10 samples. A mean CW optical power of >42.5 mW is obtained.



(a) (b)

Figure 5-1: (a) CW optical power vs. current injection, and
(b) Distribution of CW optical power at 0.35 A

5.2.1.2 The I-V characteristics of the TOSA samples are shown in Fig. 5-2. The mean operating voltage at 0.35 A drive current is 1.38 V.

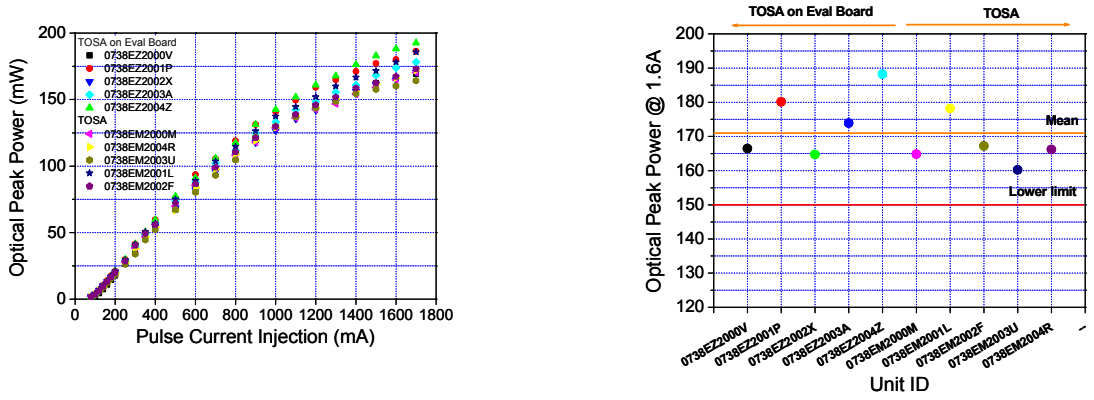


(a) (b)

Figure 5-2: (a) Forward voltage vs. current injection, and
(b) Distribution of forward voltage at 0.35 A

5.2.2 *Pulsed Optical Power and Current Drive*

5.2.2.1 The pulsed performance of the TOSA samples are characterized with the Keithley pulse driver, integrating sphere and dual photodiode meter. Measurement is carried out at 25 °C T_{SLED}, with pulse width of 2 µs and duty ratio of 0.1%. Figure 5-3 shows the measured pulsed optical power performance. The mean optical peak power obtained is 170 mW at 1.6 A current drive.

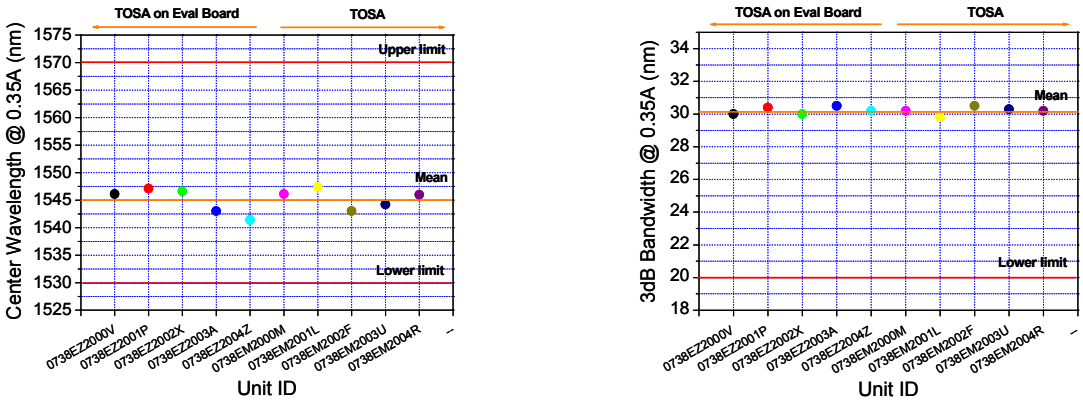


(a) (b)

Figure 5-3: (a) Optical peak power vs. pulse current injection, and
(b) Distribution of optical peak power at 1.6 A

5.2.3 *Optical Spectrum*

5.2.3.1 The optical spectrum of the TOSA samples are measured with an optical spectrum analyzer under CW operation at 0.35 A current injection and T_{SLED} of 25 ºC. As shown in Fig. 5-4, all samples have a mean center wavelength of 1545 nm and a 3dB optical bandwidth of 30 nm, demonstrating the targeted incoherent optical spectrum emission.

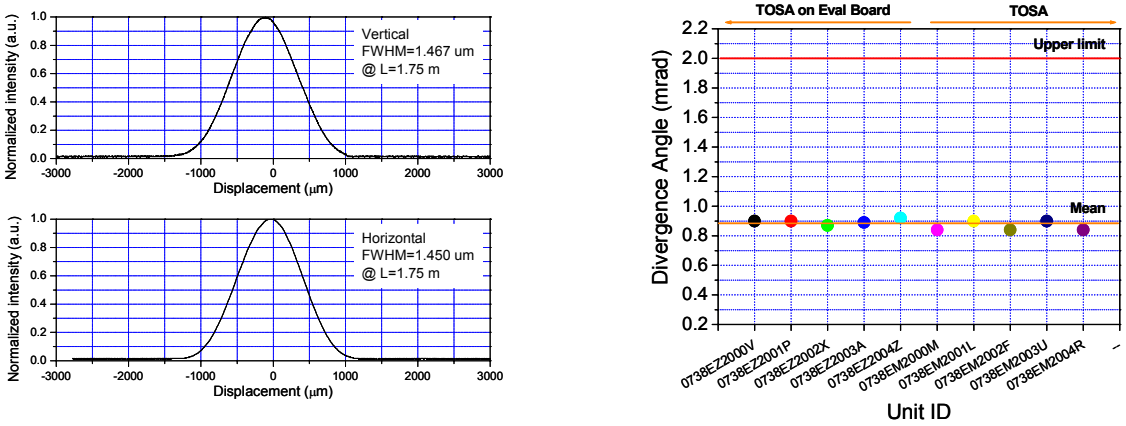


(a) (b)

Figure 5-4: (a) Distribution of center wavelength at 0.35 A, and (b) Distribution of 3dB bandwidth at 0.35 A

5.2.4 *Beam Divergence*

5.2.4.1 The TOSA light source beam divergence is measured by scanning the 2D far-field beam profile at a distance of 1.75 m from the emission point. The measured beam diameter is then used to compute the beam divergence. Figure 5-5 shows that a beam divergence of ~0.9 mrad is obtained for all the ten TOSA samples when driven at 0.35 A CW and 25 ºC.

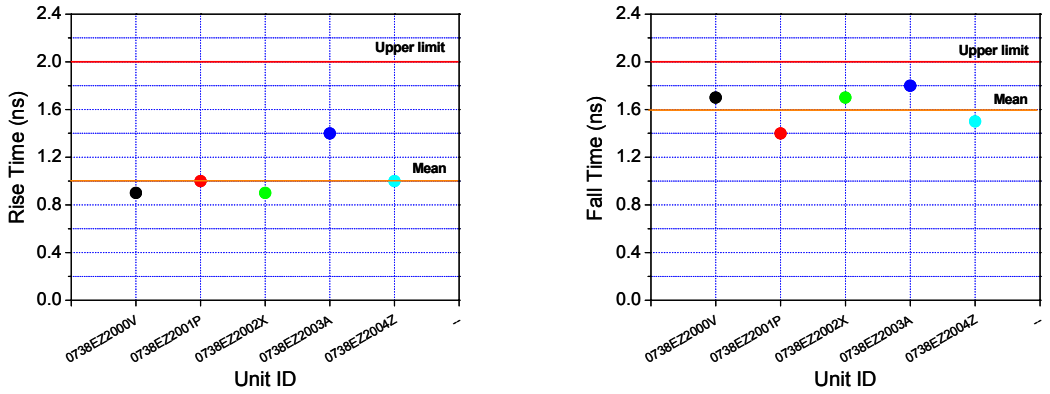


(a) (b)

Figure 5-5: (a) Measured far-field optical mode profile, and (b) Distribution of divergence angle

5.2.5 *Pulse Characteristics*

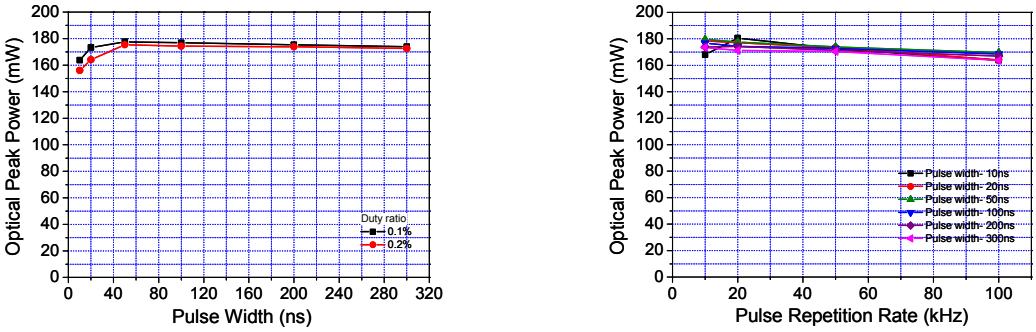
5.2.5.1 The rise and fall times of the TOSA samples mounted on DenseLight DL-US551502G-L01-Eval evaluation board are measured under operating condition of 10 ns pulse width, 0.1% duty ratio and 25 ºC T_{SLED}. Figure 5-6 shows the distribution of the rise and fall times and average values of 1.0 ns and 1.6 ns are obtained respectively. Based on earlier results discussed in section 4.4, the measured values could be limited by non-optimized tuning of the evaluation board onto which the TOSA samples are mounted.



(a) (b)

Figure 5-6: Distribution of (a) rise time and (b) fall time of TOSA mounted onto evaluation board

5.2.5.2 The dependence of the measured optical peak power with respect to the pulse width and pulse repetition rate are shown in Fig. 5-7. As can be observed, the optical peak power is independent of pulse width and pulse repetition rate, and stays at 170 mW.

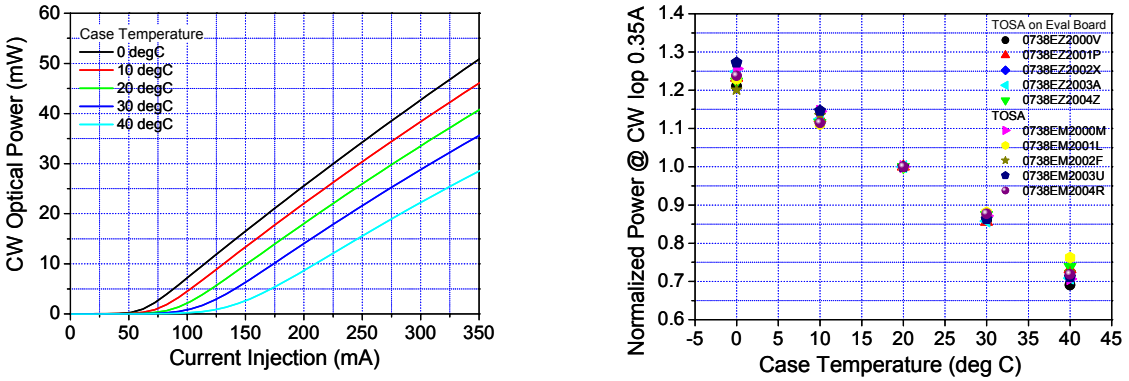


(a) (b)

Figure 5-7: Dependence of optical peak power with (a) pulse width, and (b) pulse repetition rate

5.2.6 *Case Temperature Dependence*

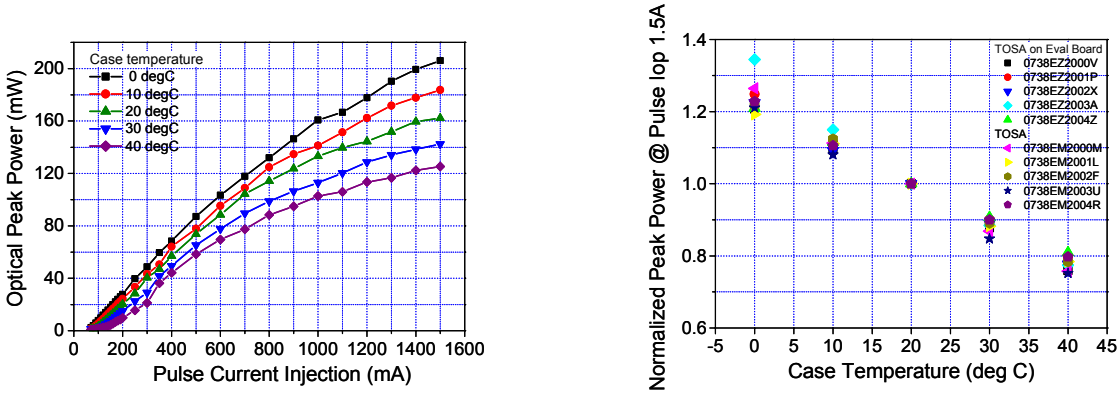
5.2.6.1 The CW optical power of the TOSA samples is measured at different SLED case temperatures from 0 to 40 ºC to ascertain the dependence of optical power with temperature. Figure 5-8 shows the measured optical power with current injection at various temperatures measured on a heatsink near to the TOSA. It can be observed that all samples exhibit similar performance and the optical power at 0.35 A drops from 50 mW at 0 ºC to ~30 mW at 40 ºC case temperature, giving an optical power sensitivity of –0.53 mW/ºC.



(a) (b)

Figure 5-8: (a) Optical power vs current injection at various case temperatures, and (b) Distribution of normalized power at 0.35 A and various case temperatures

5.2.6.2 The optical peak power of the TOSA samples is similarly characterized over 0 to 40 ºC SLED case temperatures, with current pulse width of 2 µs and duty ratio of 0.1%. Figure 5-9 shows the measured results, whereby the optical peak power sensitivity at 1.5 A drive to the case temperature is determined to be –2 mW/ºC.



(a) (b)

Figure 5-9: (a) Optical peak power vs pulse current injection at various case temperatures, and (b) Distribution of normalized peak power at 1.5 A and various case temperatures

5.2.6.3 The TOSA optical spectrum characteristics at different case temperatures have also been measured, and the results are shown in Fig. 5-10. The center wavelength increases from 1532.5 nm to 1555.0 nm when case temperature increases from 0 to 40 ºC, showing a temperature dependence of 0.56 nm/ºC. The 3dB optical bandwidth similarly increases from 26.3 nm to 33.8 nm for the 40 ºC temperature rise, or a sensitivity of 0.19 nm/ºC.

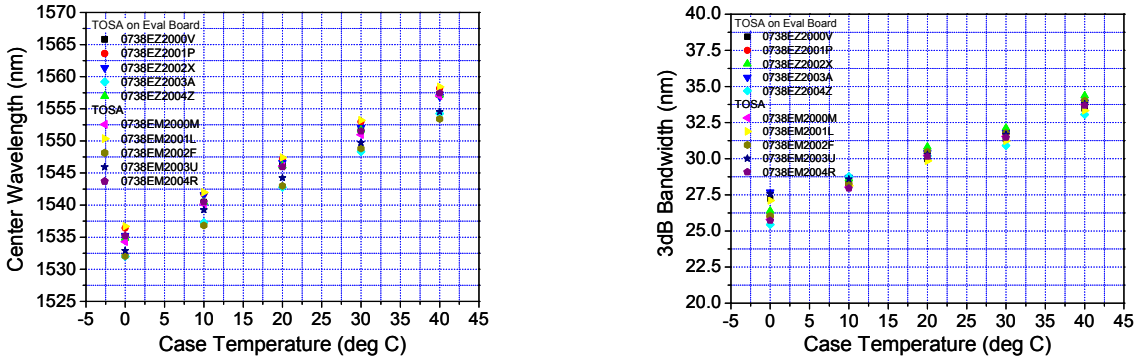


Figure 5-10: (a) Center wavelength vs case temperature, and
(b) 3dB bandwidth vs case temperature at 0.35 A current drive

5.3 Summary

5.3.1 Ten units of SLED TOSA samples have been assembled and fully tested, with 5 of the TOSA units mounted onto the evaluation board. The measured performance of the samples meets all the requirements as defined in the specifications sheet in the Appendix, and performance variation among the different TOSA samples is small. This demonstrates the good repeatability and control of the production and assembly processes.

6. Extension to Other Applications

6.1 Active Hyperspectral Imaging

6.1.1 *Background*

6.1.1.1 Electro-optical remote sensing involves acquisition of information about an object or scene without coming into physical contact with that object or scene. Recently, passive imaging has evolved beyond one panchromatic band (grey scale), or three visible color bands, to several tens to hundreds of spectral bands covering the visible spectrum, near-infrared (NIR) and shortwave infrared (SWIR) bands.

6.1.1.2 In general, hyperspectral imaging refers to taking data in many, often contiguous wavelength bands, while multispectral imaging uses just a few wavelength bands, which may be separated from each other. Essentially, these imaging techniques exploits the fact that materials comprising various objects in a scene reflect, scatter, absorb and emit electromagnetic radiation in ways characteristic of their molecular composition and macroscopic scale and shape. With the radiation arriving at the sensor measured at many wavelengths, over a sufficiently broad spectral band, the resulting spectral signature, or spectrum, can be used to identify the materials in a scene and discriminate among different classes of materials.

6.1.1.3 Typically, spectral imaging systems operate at visible through near-infrared wavelengths by relying on solar illumination. For many applications, the dependence on the measurement conditions can complicate analysis, making it difficult to compare spectral data taken under different conditions.

6.1.1.4 Actively illuminating the scene of interest offers a way to address the measurement condition dependencies while providing additional advantages. Active illumination enables a sensor to operate day or night, even under adverse weather conditions when solar illumination is greatly reduced. In addition, placing the illumination source on the sensor platform provides a constant angle between the source, target and sensor, eliminating illumination-angle variations that can complicate analysis and degrade performance. An active source also reduces shadowing, which reduces false-alarm rates.

6.1.1.5 Active spectral imaging can be applied to the detection of various types of military targets, such as inert land mines and camouflage paints and fabrications, using a combination of spectral reflectance, fluorescence and polarization measurements.

6.1.2 *SWIR Band and Application of SLED Illumination*

6.1.2.1 It is known the water-vapor absorption lines in the SWIR can be exploited as sources of contrast to distinguish between natural and man-made objects. Man-made objects, particularly paints and plastics, tend to be hydrophobic; they are designed to repel water to prevent rust, corrosion and degradation. Natural materials tend to be hydrophilic; they retain water because they are either porous (in the case of rocks and soils) or living (in the case of vegetation). Consequently, natural objects like rocks and foliage typically absorb more radiation in the 1.4 µm and 1.9 µm water-vapor absorption lines

than do man-made objects. By taking a simple ratio of two broad SWIR spectral bands, one can achieve good anomaly-detection performance and distinguish man-made objects from natural objects.

6.1.2.2 The reflected SWIR light from the scene can be imaged using InGaAs based cameras, and it is not detectable to the human eye, night vision goggles or silicon cameras. This hence offers the additional advantage of covertness from detection by the common imaging technologies.

6.1.2.2 Based on similar InGaAsP/InP material system, the SLED chip, TO-can and TOSA compact platform design methodologies developed in this program could be extended to enable speckle-free SLEDs illuminators in the wavelength range of 1250 nm to 1650 nm with high brightness and low divergence. A set of SLED TOSA units of selected wavelengths could be mounted in a carousel surrounding the camera imaging sensor to realize an active SWIR hyperspectral imaging system.

6.2 Underwater Diver Communications

6.2.1 *Background*

6.2.1.1 With the increased diving activities for various underwater applications and engagements, reliable communications between all personnel involved with the dive operation is essential. This includes communications with the actual divers and also coordination with supervisory topside, life support and tender personnel.

6.2.1.2 Scuba divers are trained to use hand signals to communicate with their buddies. They also use underwater writing boards, which allow for better communication. However, both of these techniques require light and will be much impaired when the water is murky, or during nighttime, or if the divers are too far apart to see one another clearly.

6.2.1.3 Special acoustics underwater communication systems have been developed to allow divers to talk to each other underwater. A transducer is attached to the diver's facemask, which converts his or her voice into an ultrasound signal. A fellow diver has an ultrasound receiver, which accepts the signal and converts it back to a sound that the diver can hear, allowing for communication. The same system can be used for communication between the diver and a surface ship. However, this is generally of low bandwidth of around several tens of kb/s, which is still sufficient for speech communication between divers and a surface station or among divers.

6.2.1.4 Free-space underwater optical transmission is a promising communications technology, which would greatly enhance the transmission bandwidth to around 10 ~ 100 Mb/s. Similar to acoustics systems, the wireless optical systems eliminate physical connection of tethers, allowing for speech communications between divers, as well as gathering of data from submerged instruments without human intervention and operation of unmanned or autonomous underwater vehicles.

6.2.2 *Underwater Optical Propagation*

6.2.2.1 Optical propagation underwater is critically dependent on water optical properties, which vary with water depth, geographic location and time of day. Organic and inorganic particulates, as well as temporal variations such as turbulence, also affect the water properties.

6.2.2.2 Intrinsic absorption of water, dissolved impurities and organic matter leads to loss of beam intensity underwater. Seawater is primarily H_2O, and has dissolved salts, such as NaCl, $MgCl_2$, Na_2SO_4, $CaCl_2$ and KCl, that absorb light at specific wavelengths. Figure 6-1 shows the absorption spectrum of pure seawater, and it is clear that pure seawater is absorptive, except for blue-green wavelength window of 400 to 530nm.

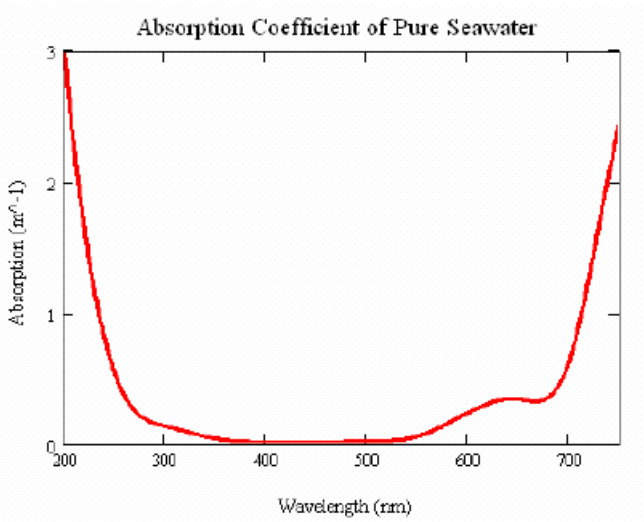


Figure 6-1: Spectral absorption coefficient of pure seawater[1]

6.2.2.3 Scattering, the redirection of incident photons into new directions, preventing forward on-axis transmission of photons, is an important phenomenon that affects underwater optical propagation. A consequence of scattering is that the optical beam will spread in diameter (increase in beam divergence) or loss light intensity (increase in attenuation).

6.2.2.4 Figure 6-2 shows the attenuation of light in different water type environments. It can be seen that closer to land where river runoff introduces particulate and organic matter, scattering dominates attenuation coefficient. Correspondingly, the attenuation coefficient shifts from blue region of ~450 nm for ocean water to more greenish region ~525 nm for coast water with worsening of water condition. This implies that the optimal optical wavelength to be used for underwater propagation depends on the water environment in which the optical transmission takes place.

[1] J. R. Apel, Principles of Ocean Physic, pp. 509-584, International Geophysics Series, vol. 38, Academic Press, 1996.

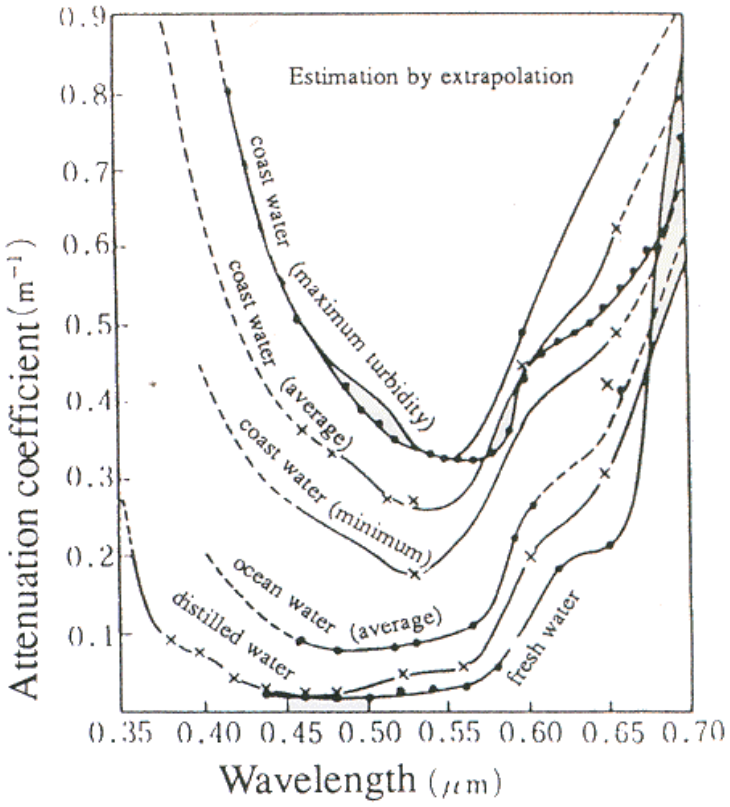


Figure 6-2: Spectral attenuation coefficient dependence on water type, turbidity[2]

6.2.3 *Compact Blue-Green Transmitter Source*

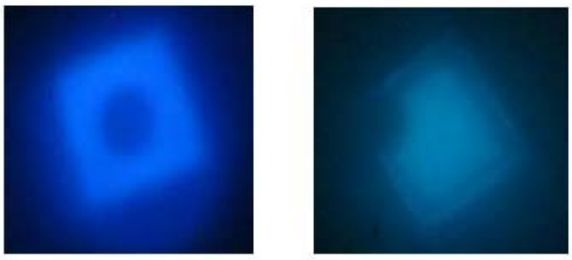
6.2.3.1 The key requirements of the transmitter source for underwater optical wireless link are:

a) emission wavelength in low absorption loss region of water
b) power scalability to W and above
c) bandwidth of >1 MHz at high power operation
d) efficient and compact optics collimation

6.2.3.2 Selection of most suitable light source for transmitter is very important. GaN based light sources of LED and LD designed for DVD application emit in wavelength range of 400 to 500nm, which matches well with low loss absorption region of water. Blue-green LEDs typically have an output power of around 70lumens or 1W and are fabricated as surface-emitting devices, resulting in poor beam divergence for long distance propagation. Figure 6-3 shows the typical blue-green LEDs and their beam profile.

[2] "Remote Sensing Note" from Japan Association of Remote Sensing, 1966.

(a)



(b)

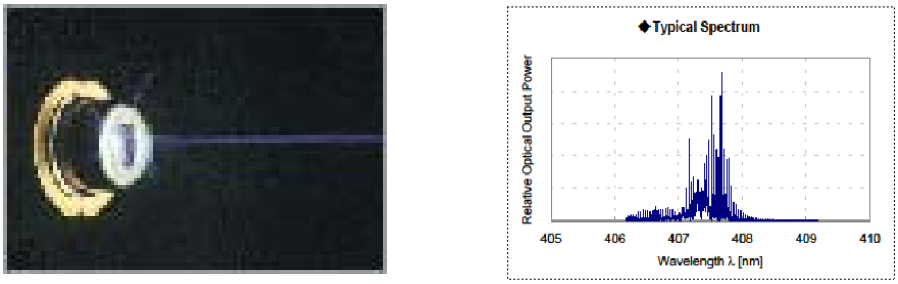
Figure 6-3: (a) Typical LED package and (b) their resultant beam emission profile (left picture is a conventional packaged LED, and right picture is Lumileds package)

6.2.3.3 The best alternative light source for underwater optical propagation is the blue-green diode laser, which currently has reached output powers of >100mW. Emission wavelengths are clustered into bands of 406nm, 445nm and 473nm, and they can be modulated above 10MHz. Table 6-1 summarizes the specifications of blue-green LD from major suppliers of Nichia, Sharp and Sony. Package form factors are in TO-56 cans shown in Fig. 6-4a, and typical lasing spectrum is shown in Fig. 6-4b.

Table 6-1: Specifications of blue-green laser diodes[3, 4, 5]

	Sony	Sharp	Nichia	Nichia	Nichia	Nichia
	SLD3233VF	GH04P21A2G	NDHV220APAE1	NDHV310APC	NDHB510APA	NDHA210APAE1
Peak wavelength	405nm	406nm	408nm	408nm	445nm	473nm
P_{opt} (CW)	65mW	105mW	200mW	60mW	50mW	20mW
I_{th}	35mA	40mA	100mA	40mA	35mA	50mA
I_{op}	80mA	110mA	230mA	85mA	120mA	100mA
V_{op}	4.9V	NA	4.2V	4.6V	5.5V	5.5V
FWHM (//)	8.5°	9°	20°	8°	8.5°	9°
FWHM (|-)	21°	19°	45°	22°	22°	23°
Operating case temp	Up to 75°C	0 ~ 70°C	TBD	-10 ~ 60°C	-10 ~ 60°C	0 ~ 60°C
Package	NA	TO-56	TO-56	TO-56	TO-56	TO-56

[3] http://www.sony.net/Products/SC-HP/pro/laser_diode/blu_ray.html
[4] http://sharp-world.com/corporate/news/070314.html
[5] http://www.nichia.com/product/laser-main.html



(a) (b)

Figure 6-4: Blue-green laser diode: (a) TO-can package, (b) optical spectrum

6.2.3.4 For underwater transmission application, the blue-green light source needs to have its optical profile tailored to low divergence for good collimation across range required. The developed TOSA compact platform in this project, which integrates an aspherical lens with the emitter chip in a TO-can, can also be extended to the blue-green light source. These blue-green TOSA modules could also be mounted in specific array configurations so as to scale up the transmitter optical power to the required level.

7. Conclusions

7.1 The indium phosphide-based SLED is an ideal light source for eye-safe target designation and imaging at 1550 nm spectral region. Its wide spectral width ensures a low coherency, which is critical for speckle free imaging. A high brightness and well-collimated output beam allow for projection of the illumination across long distances.

7.2 In this project, DenseLight Semiconductors designed, developed and demonstrated a high brightness SLED chip that exceeds 200 mW in peak optical power output and >20 nm of spectral bandwidth at 1550 nm wavelength. This optical power level is the highest value ever achieved, exhibiting more than 2 times improvement over baseline SLED chips operating in the same wavelength range.

7.3 The SLED chip is packaged into a compact 7-pin TO-8 platform with built-in collimating aspherical lens. The packaging design and process development of this transmitter optical sub-assembly (TOSA) achieved a very low beam divergence of 1 mrad.

7.4 In addition, the SLED chip and TOSA package are designed for both high optical power and high-speed pulse operation. An optical pulse stream of 10 ns pulse width, 0.1% duty ratio and rise and fall times of 1 ns has been demonstrated, allowing for high speed pulsed illumination applications.

7.5 In follow on efforts, the chip and packaging design concept implemented in this project could be extended to SLEDs emitting in other wavelengths, which would serve as key enabling optical components for hyperspectral imaging applications, as well as to blue-green laser diodes as transmitter source for underwater communications among divers.

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SPECIFICATIONS

1550 nm SWIR SLED-TOSA: Short Wavelength Infrared Superluminescent Light Source

DL-US551502G-L01

A. PRODUCT DESCRIPTION

The DenseLight DL-US551502G-L01 series is a 1550nm SWIR-SLED (Short-Wavelength-Infrared Superluminescent LED) all-semiconductor high brightness and speckle-free light source packaged in a TO-8 TOSA, intended for applications in long range IR illumination. It is suitable for use in conjunction with IR focal plane arrays to realize a covert IR camera illuminator, since conventional silicon-based CCD imaging sensors and FLIR infrared cameras are not sensitive to illumination at this wavelength window.

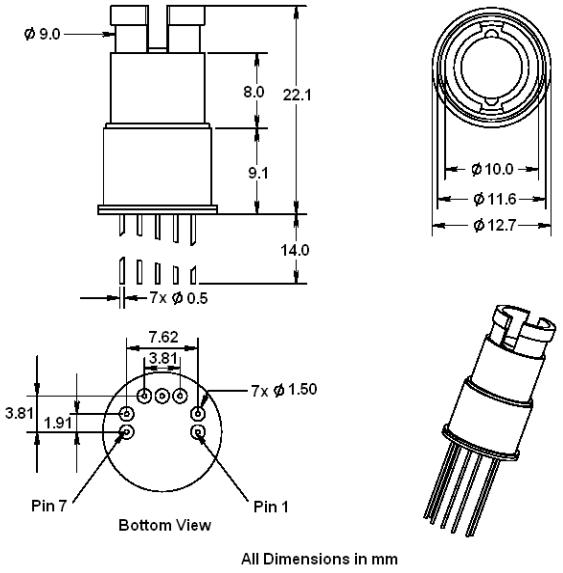
This DL-US551502G-L01 is integrated with optical collimating lens to provide excellent low divergence output light beam and is capable of being direct intensity modulated at high speed or to operate in quasi-CW modes.

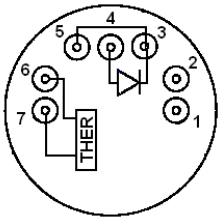
For responsive prototyping enquiries please email: info@denselight.com

B. FEATURES

- Optical peak power of >150mW
- Center wavelength of 1550nm
- 3dB spectral bandwidth of >20nm
- Modulation rise time & fall time of 1ns (Typ)
- Optical divergence <2mrad
- 7-pin TO-8 TOSA (Transmitter Optical Sub-Assembly)
- Operating temperature range 0 to 40°C

C. PACKAGE





Pin Assignment	Description
1	N/C
2	N/C
3	SLED Cathode (-)
4	SLED Anode (+)
5	SLED Cathode (-)
6	Thermistor
7	Thermistor

D. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min	Max	Unit
Reverse voltage	V_R			2	V
Forward voltage	V_F	I_{op}		3.5	V
Forward current	I_F	Pulse[1]		1.8	A
Case temperature	T_C	I_{op}	0	40	°C
SLED temperature[1]	T_{SLED}	I_{op}	0	70	°C
Storage temperature	T_{stg}	Unbiased	-40	85	°C
Storage humidity			5	85	%RH
Electro static discharge (ESD)	V_{ESD}	Human body model		500	V
Lead soldering temperature	S_{temp}			260	°C
Lead soldering time	S_{time}			10	sec

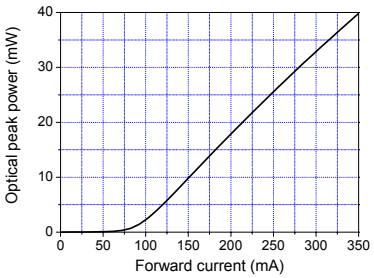
E. SPECIFICATIONS (T_{SLED}[1] = 25 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Forward voltage	V_F	CW			3.0	V
Forward current	I_F	Pulse[2]			1.6	A
		CW			0.35	
Optical power	P_{peak}	Pulse[2]	150			mW
	P_o	CW	35			
Modulation rise time and fall time	t_r & t_f	Pulse[2]		1	2	ns
Center wavelength	λ_c	CW	1535	1550	1565	nm
3dB Spectral width	B_{FWHM}	CW	20			nm
Divergence angle	$\theta_{divergence}$	CW			2	mrad
Thermistor resistance	R_{therm}	T = 25 °C	9.5	10	10.5	kΩ

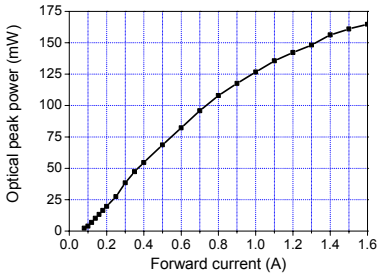
1 T_{SLED} is monitored by internal thermistor with external pin out.
2 Pulse condition: Pulse width, tpw=10ns, Duty ratio= 0.1%

F. TYPICAL PERFORMANCE CHARACTERISTICS

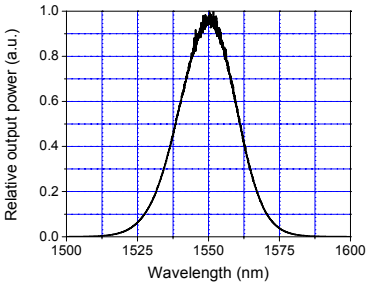
Operating condition: T_{SLED}= 25 °C



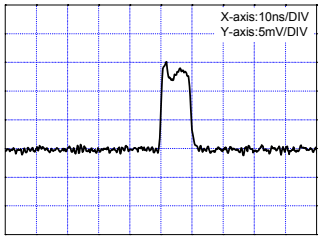
Power vs. Forward Current
CW



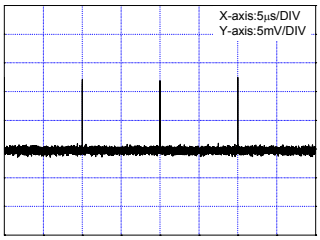
Power vs. Forward Current
tpw=10ns, duty ratio=0.1%



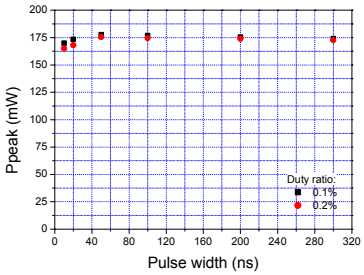
Optical Spectrum
CW: I_F=0.35A



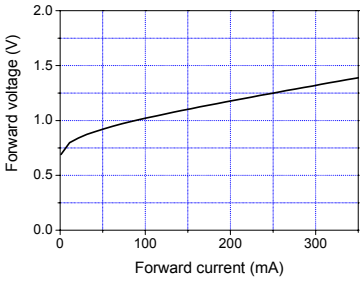
Scope Trace of One Pulse
Pulsed: tpw=10ns, duty ratio=0.1%



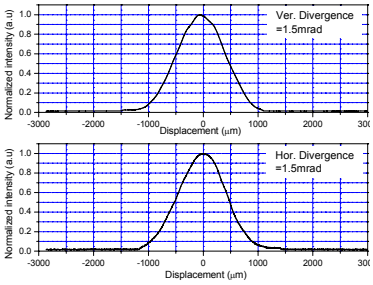
Scope Trace of Pulse train
Pulsed: tpw=10ns, duty ratio=0.1%



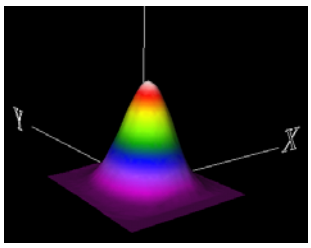
Peak Power vs. Pulse width



Forward Voltage vs. Forward Current
CW



Plot of divergence
CW: I_F=0.35A



3D plot of divergence
CW: I_F=0.35A

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SPECIFICATIONS

Evaluation Board for 1550 nm DL-CS551502G-L01 Series of 1550nm SWIR-SLED-TOSA Short Wavelength Infrared Superluminescent LED

DL-CS551502G-L01-Eval

A. PRODUCT DESCRIPTION

The DenseLight DL-CS551502G-L01-Eval evaluation board is designed to offer a platform for customers to evaluate the DL- CS551502G-L01 Series of 7-pin TO-8 TOSA 1550nm SWIR light source, which is intended for long range IR illumination. The board is complete with the SWIR-SLED device and the essential drive electronics to support a comprehensive range of testing with minimal external electronics instrumentations. The evaluation unit shows an example of how the SWIR-SLED can be clamped on the evaluation board for thermal dissipation, with short leads for low-inductance high-speed pulse driving of the SLED light output over various range of power levels, pulse width and pulse repetition rate. It should be used in conjunction with the DL-CS551502G-L01data sheet, which contains detail specification.

For quick responsive prototyping enquiries please email: info@denselight.com

B. FEATURES

- Use simple laboratory power supplies (+7V, +9V)
- Mounting clamp for SWIR-SLED unit
- Preset for 0-2A variable pulse current
- Simplified test electronics interface (high speed current pulse generator on board)
- Preset for 10ns to 300ns pulse width (<2ns rise/fall times)
- User defined pulse repetition rate/pattern via external trigger input (CMOS/TTL-logic)
- Built-in temperature controller with preset chip operating temperature from 0 to 40 °C

C. RELATED DOCUMENT

DenseLight DL-CS551502G-L01 7-pin SWIR-SLED-TOSA 1550nm IR light source

D. EVALUATION BOARD LAYOUT

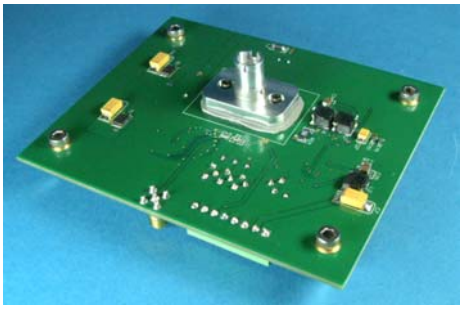


Figure 1A. Evaluation board bottom-side where the TO-8 TOSA SWIR light source is mounted

Figure 1B. Evaluation board top side where most of the electronic components are mounted

E. PHYSICAL DIMENSIONS AND MECHANICAL SPECIFICATION

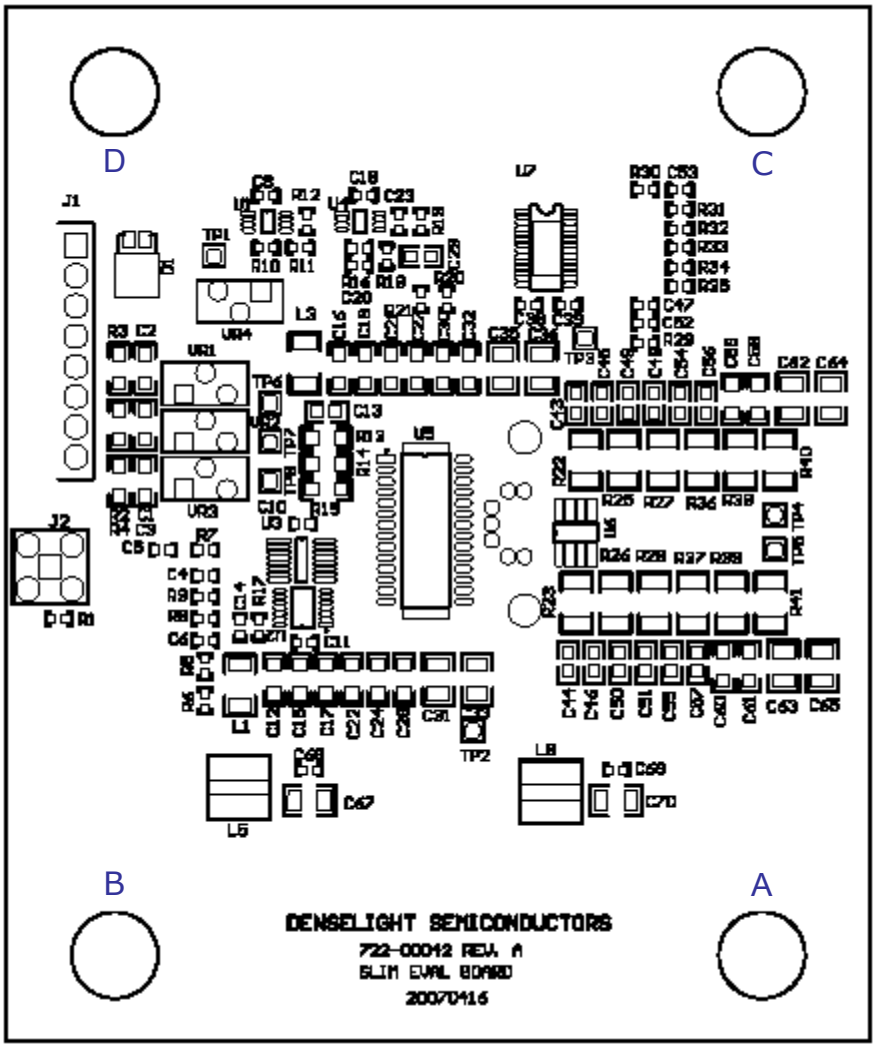


Figure 2a. Top Side Mechanical Layout

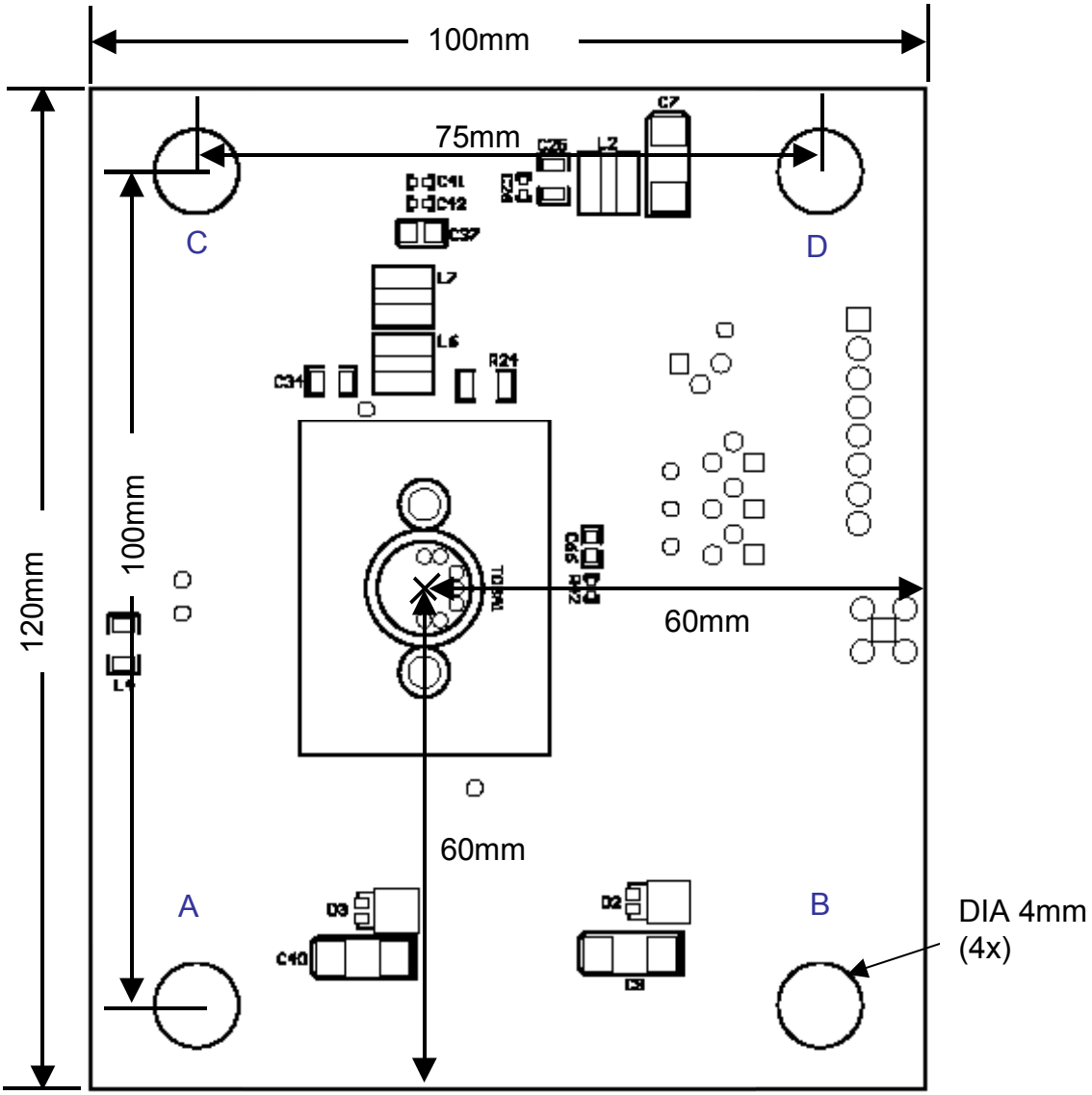


Figure 2b. Bottom Side Mechanical Layout*

* a) Orientation to Top-Side: Reference board mounting holes identifiers A, B, C, D
b) SWIR-SLED light emitting point is identified by “X”

F. PIN ASSIGMENT AND FUNCTION

Label	Connector Type	Pin No.	Description
J1	8-pin Header	1	NC
		2	NC
		3	Power supply ground
		4	+7V D.C.
		5	Power supply ground
		6	+9V D.C.
		7	NC
		8	NC
J2	SMA		External Trigger Input (CMOS/TTL compatible)
TP1	Test Point Connector		-
TP2	Test Point Connector		GND
TP3	Test Point Connector		GND
TP4	Test Point Connector		To monitor light source Anode voltage
TP5	Test Point Connector		To monitor light source Cathode voltage
TP6	Test Point Connector		To monitor voltage across VR1 that control the current I_{IBI}, flowing into IBI pin of IXLD02** high-speed LD driver IC that used as a baseline current with respect to I_{IPW} current to compensate for internal delays
TP7	Test Point Connector		To monitor voltage across VR2 that control the current I_{IOP}, flowing into IOP pin of IXLD02 high-speed LD driver IC that used to tune the LD current
TP8	Test Point Connector		To monitor voltage across VR3 that control the current I_{IPW}, flowing into IPW pin of IXLD02 high-speed LD driver IC that used to tune the LD current pulse width

Note:
**Refer to data sheet of IXLD02 at www.directedenergy.com/poudcts/ics.htm

Caution: Do not apply reverse voltage to pins as this might cause permanent damage to the evaluation board

G. MEASUREMENT SETUP

G.1 Equipment used for measurements:

1. Agilent 33250A Function generator
2. Tektronix TDS3052B Oscilloscope
3. Three Topward 3306D DC power supplies
4. Fluke 179 Multimeter
5. New Focus 1414 high-speed photodetector (FC connectorized)
6. Thorlabs F810FC-1550 fiber collimator
7. Keithley Integrating sphere 2500INT-2-IGAC and 2500 dual photodiode meter
8. Single mode fiber (SMF-28) 1m with FC/APC termination
9. Matched high-speed cables with SMA (50 Ohm) connectors
10. BNC cables with 50 Ohm termination

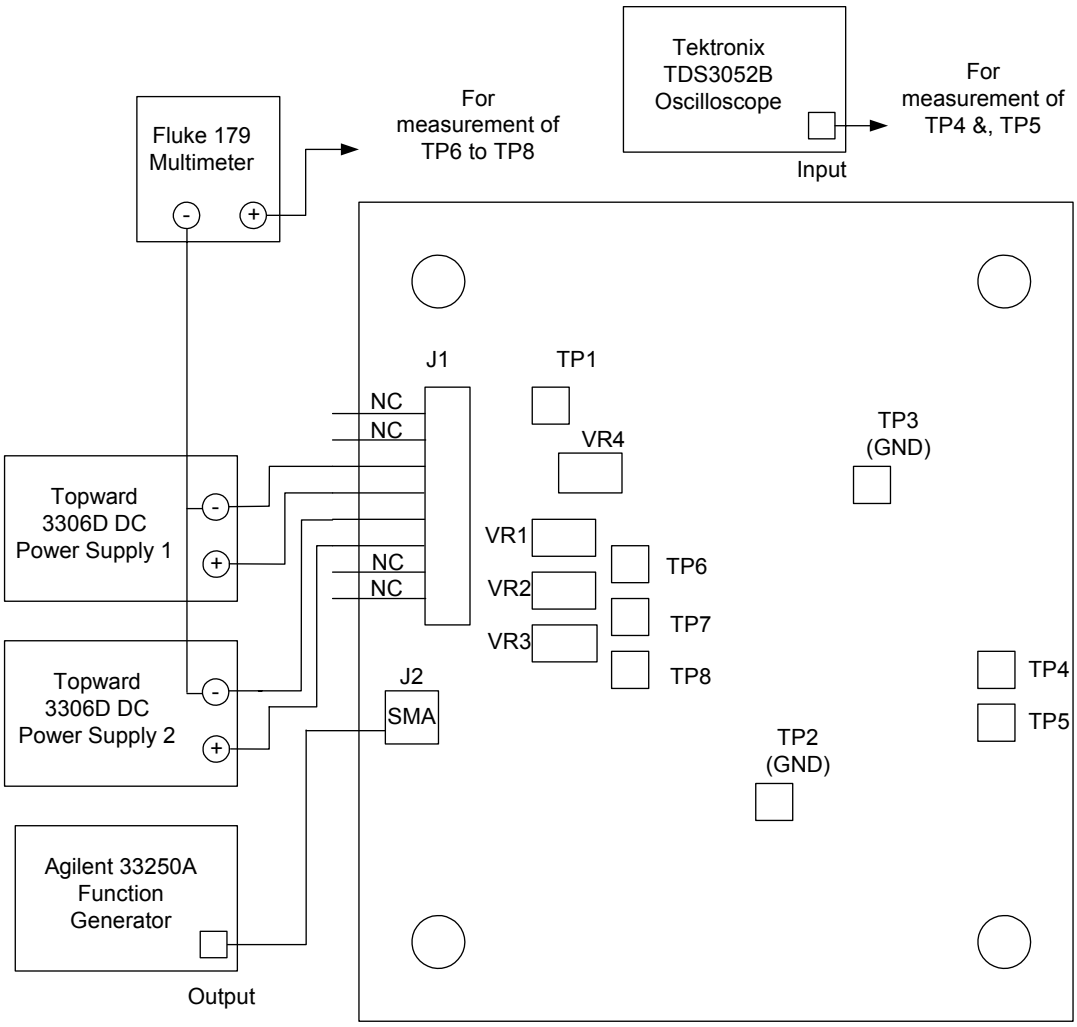


Figure 3a. Power supply connection setup

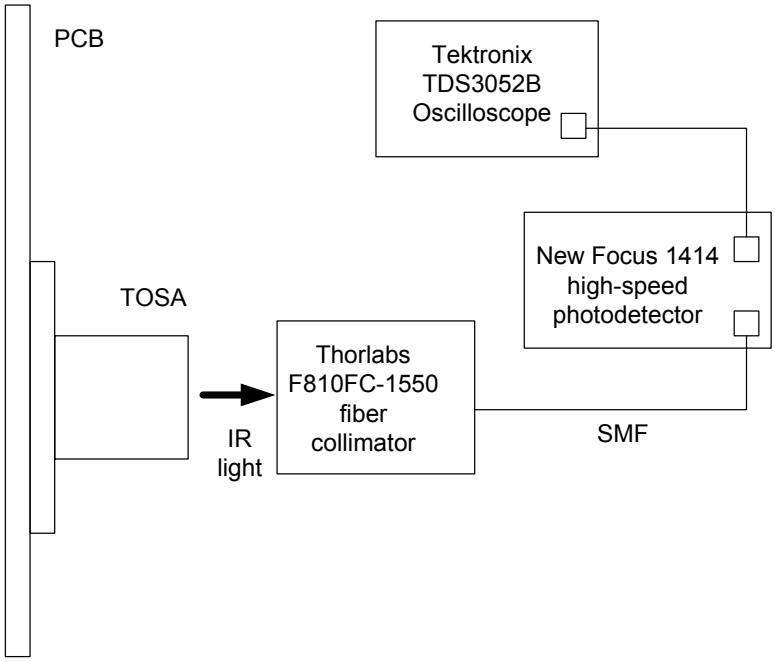


Figure 3b. Optical light source signal measurement setup

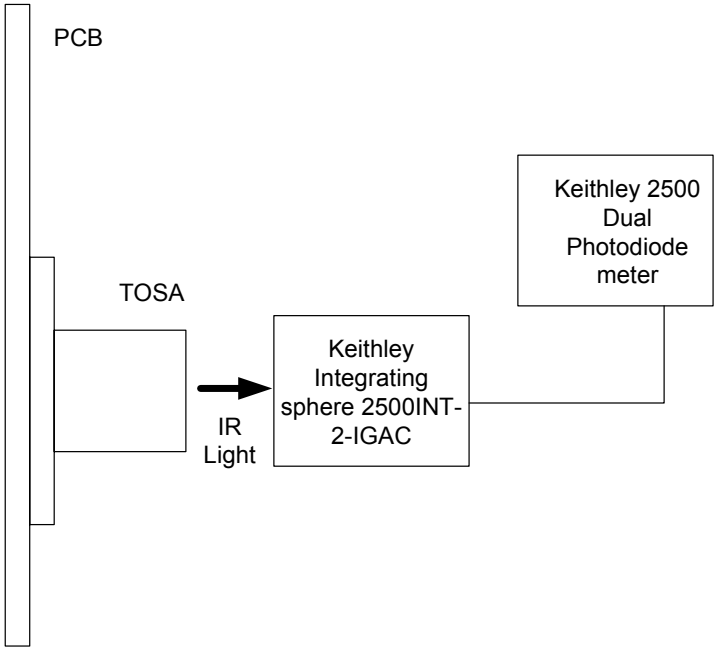


Figure 3c. Optical light source power measurement setup

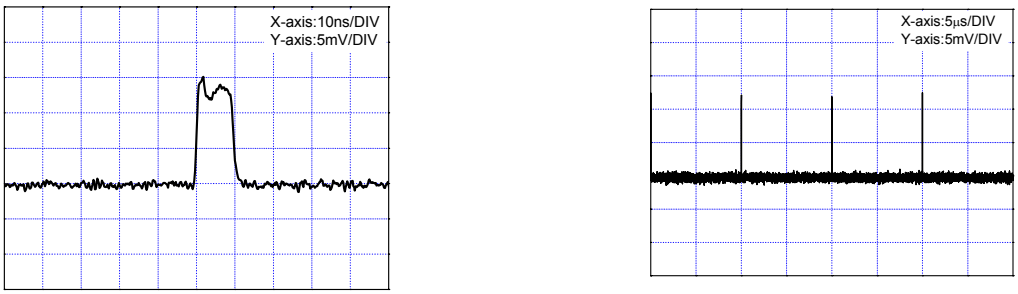
G.2. Setup for Measurements:

This section explains the procedure to connect and setup the DL-US551502G-L01 series evaluation board as shown in Figure 3a to 3c. Ensure proper **Electrostatic Discharge (ESD)** precautionary measures are taken before handling the evaluation board and sensitive electronic equipment. The IR light source meets the calculated **AEL Class 3R** limits. Precautionary care has to be taken to avoid continuous viewing of the direct beam. Adequate eye protection against laser radiation should be used while handling and operating the device.

Default Factory Setup:

1. Set Topward 3306D DC Power Supply 1 to 7V output and 1A current limit. Connect J1-3 to the negative terminal and J1-4 to the positive terminal. Turn on the DC Power Supply 1 and this will power up the LD driver of the evaluation board.
2. Set Topward 3306D DC power supply 2 to 9V and 1A. Connect J1-5 and J1-6 to the negative and positive terminal. Turn on the DC Power Supply 3. Set the Agilent 33250A function generator with square pulse of amplitude=2Vp-p, frequency=100kHz and Pulse width=500ns (TTL/CMOS logic levels). Connect the signal output from J2 (SMA) to the output of the function generator and this will turn on the IR light source.
3. Guide the collimated light output from the SWIR light source into the New Focus 1414 high-speed photodetector using the Thorlabs F810FC-1550 fiber connector. Connect the monitor output to the input of the Tektronix TDS3052B Oscilloscope using matched high-speed cable. Refer to Figure 3b for the measurement setup. Measure the following parameter from the oscilloscope:
    i) Rise time and fall time
    ii) Pulse width
    iii) Pulse repetition rate

    A typical trace of pulse is shown in Figure 4. Measure TP6, TP7 and TP8 using Fluke 179 multimeter. The reading should be similar to the value recorded in measurement report attached during shipment. Fine-tune the pulse width by adjusting the VR3 if it varies from the setting. To measure the voltage across the SWIR light source, obtain the voltage difference between TP4 (TP3 as GND) and TP5 (TP2 as GND) using Tektronix TDS3052B Oscilloscope. The reading should be ~2 to 3V.
4. Refer to Figure 3c for the measurement setup of optical power output. Guide the light directly into the Keithley Integrating sphere 2500INT-2-IGAC and read the photocurrent from Keithley 2500 dual photodiode meter. The peak pulse power is >150mW.



(a) (b)

Figure 4. Scope trace of (a) Single pulse (b) Pulse train, with pulse width=10ns and repetition rate =100kHz.

LD Current Pulse Width Tuning:

The pulse width of the current that drive the SWIR light source can be tuned via variable resistors VR1 and VR3. VR1 controls the current I_{IBI}, flowing into IBI pin of IXLD02 high-speed LD driver IC that is used as a baseline current with respect to I_{IPW} current to compensate for internal delays. Whereas, VR3 controls the current I_{IPW}, flowing into IPW pin of IXLD02 high speed LD driver IC that is used to tune the SWIR light source current pulse width. Turning the VR1 and VR3 in clockwise direction will reduce the I_{IBI} and I_{IPW}, while anti-clockwise will increase both values. The voltage across VR1 and VR3 can be monitored via TP6 and TP8 respectively. The value of I_{IBI} should be higher than I_{IPI}. If I_{IPW}=I_{IBI}, the pulse width is 0. As I_{IPW} approaches I_{IBI} but less than I_{IBI}, the pulse width becomes smaller. Figure 5 illustrates the relationship of current pulse width t_{PW} versus I_{IPW} with respect to I_{IBI}.

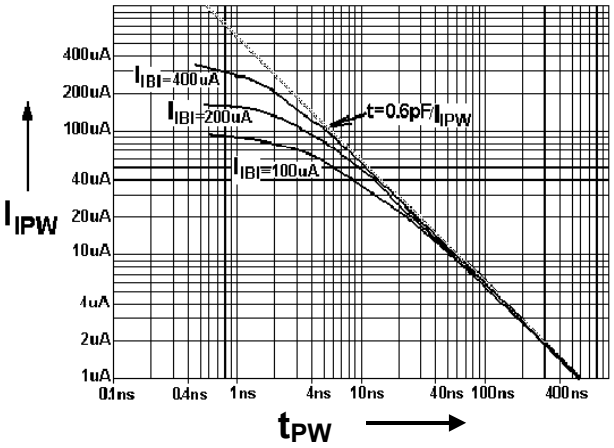


Figure 5. Current pulse width versus IPW current (Abstracted from page 5 of IXL02 Ultra high-speed laser diode driver IC specification from Directed Energy Inc)

LD Current Tuning:

The output current that drive the SWIR light source can be tuned via variable resistors VR2. VR2 controls the current IIOP, flowing into IOP pin of IXLD02 high-speed LD driver IC that is used to tune the driving current. The voltage across VR2 can be monitored via TP7, while the voltage across the IR light source can be obtained from the measurement of voltage difference between TP4 (TP3 as GND) and TP5 (TP2 as GND) using Tektronix TDS3052B Oscilloscope.

H. BILL OF MATERIALS

Item	Part number	Manufactuerer	Description	Qty
U2	SN74AHC08PW	Texas Instruments Incorp.(1)	AND Gates, TSSOP-PW-14	1
U3	LT1721CGN	Linear Technology Corp.(2)	Comparator, SSOP-DBQ-16	1
U5	IXLD02SI	Direct Energy Inc (3)	High speed LD driver IC, SO28	1
U6	GS8DI25104	IXYSRF (4)	Schottky diode, SOIC-DEI-8	1
D2 D3	PDS760	Diodes Incorporated (5)	Schottky barrier rectifier, POWERDI5	2
R9			0 Ohm resistor, 603	1
R5			1k Ohm resistor, 603	1
R6			3.9k Ohm resistor, 603	1
R17			10 Ohm resistor, 603	1
R1			49.9 Ohm resistor, 603	1
R7			510 Ohm resistor, 603	1
R8			620 Ohm resistor, 603	1
R42			909 Ohm resistor, 603	1
R13 R15			20k Ohm resistor, 1206	2
R14			3.3k Ohm resistor, 1206	1
R2 R3 R4			3.3 Ohm resistor, 1206	3
R22 R23 R25 R26 R27 R28 R36 R37 R38 R39 R40 R41			20 Ohm resistor, 2010	12
VR1 VR2 VR3			1k Ohm Variable resistor, PV36Y	3
C4 C10 C11			0.1uF Capacitor, 603	3
C68 C69			0.47uF Capacitor, 603	2
C14			1nF Capacitor, 603	1
C5 C6			0.01uF Capacitor, 603	2
C43 C44 C45 C46 C48 C49 C50 C51			0.01uF Capacitor, 805	8
C13 C54 C55 C56 C57			0.1uF Capacitor, 805	5
C66			0.47uF, 50V Capacitor, 805	1
C1 C2 C3 C12 C15 C16 C17 C19 C21 C22 C24 C27 C28 C30 C32 C58 C59 C60 C61			0.47uF, 50V Capacitor, 1206	19
C31 C33 C35 C36 C62 C63 C64 C65 C67 C70			10uF, 16V Capacitor, 1210	10
C9 C40			330uF, 16V Capacitor CASE_D	2
L1 L3 L4	BLM41PG181SN1	Murata Manufacturing Co.(6)	EMI Suppression Filter, 1806	3
L5 L8			10uH Inductor, CDRH6D28	2
J1	SL 3.5/8/90G	Weidmuller (7)	Header 8, 8-PIN CON - 1937554	1
J2			SMA	1

Notes:

1. Texas Instruments Incorp.: www.ti.com
2. Linear Technology Corp.: www.linear.com
3. Directed Energy Inc: www.directedenergy.com
4. IXYSRF: www.ixysrf.com
5. Diodes Incorp.: www.diodes.com
6. Murata Manufacturing Co.: www.murata.com
7. Weidmuller: www.weidmuller.com

Short-Wavelength-Infrared Superluminescent LED

TO-8 TOSA

User Operation Manual

Doc#: 418-0041-01-004-07-001
8 September 2007, Rev A

CONTENTS

DISCLAIMER

Read though this manual carefully before using the Short-Wavelength-Infrared Superluminescent LED (SWIR-SLED).

DenseLight Semiconductors Pte Ltd is not liable in any way for damages or injuries that may result from the use or misuse of this product. Upon purchase and receipt of this product the customer is entirely responsible for any personal or property damage that may result from the use or misuse of this product.

1. OPERATION SPECIFICATION

1.1 Absolute Maximum Ratings

Refer to the specifications and the outgoing testing report attached to the SWIR-SLED. Do not operate or expose the SWIR-SLED to extreme conditions exceeding the specified absolute maximum ratings.

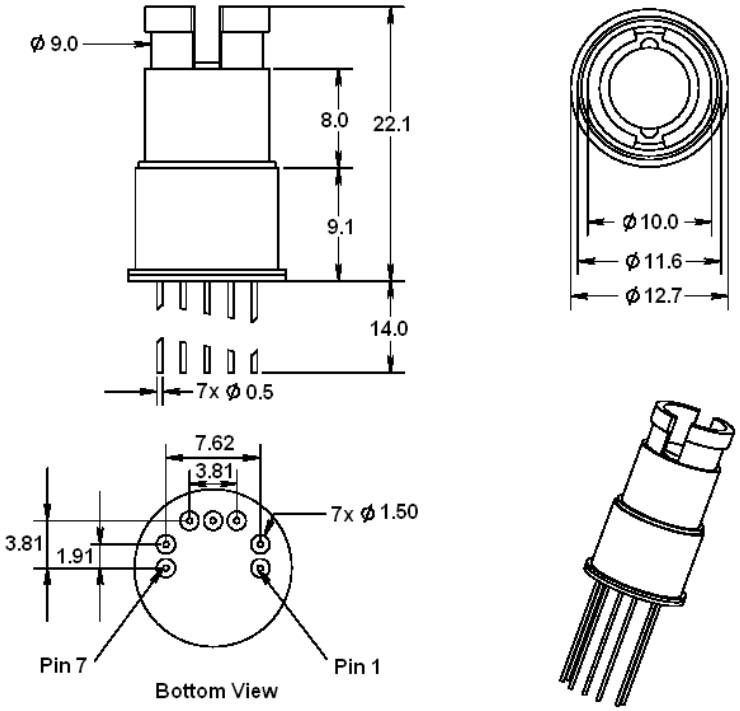
Caution: Operating beyond the absolute maximum ratings may cause permanent damages to the device. Exposure to absolute maximum rating condition for extended periods may affect device reliability. DenseLight declines any responsibilities of the damages arising from operating beyond the absolute maximum ratings specified for each model, unless otherwise agreed by DenseLight in writing.

1.2 Optical/Electrical Specification

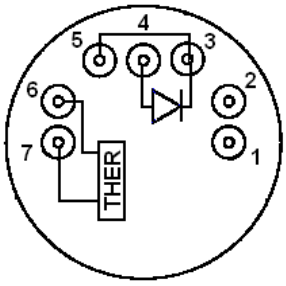
Each SWIR-SLED is tested and meets the requirements at the specific conditions as specified for each model.

Caution: Use of device other than those specified herein and within instruction manual may result in hazardous laser radiation exposure.

2. PACKAGE TYPE



All Dimensions in mm



Bottom View

Pin Assignment	Description
1	N/C
2	N/C
3	SLED Cathode (-)
4	SLED Anode (+)
5	SLED Cathode (-)
6	Thermistor
7	Thermistor

Note: Specification and drawings described in this publication are to be considered illustrations in nature and not to scale. DenseLight reserves the rights to change the specifications without prior notice.

3. EYE SAFETY CLASSIFICATION

The SWIR-SLED meets the calculated AEL Class 3R limits. Precautionary care has to be taken to avoid continuous viewing of the direct beam.

Adequate eye protection against laser radiation should be used while handling and operating the device.

Note: Class3R is defined as hazardous under direct and specula reflection viewing, diffuse reflection usually not hazardous, normally not a fire hazard and CW upper limit is 0.5W.

4. ELECTROSTATIC DISCHARGE

The SWIR-SLED is an Electrostatic Discharge (ESD) sensitive component and should be handled in static safe area.

Grounded wrist strap is to be worn at all times when manually handling the SWIR-SLED.

In operating SWIR-SLED, sufficient surge protection measures are required. Surge current is easily generated during power ON/OFF and output adjustment.

5. THERMAL MANAGEMENT

The SWIR-SLED is operated without thermoelectric cooler (TEC). It shall at no time be operated without proper heat sinking. The selection of the heatsink depends on the SWIR-SLED model and the actual application, with the consideration of thermal load and the ambient temperature as well as the convection. The SWIR-SLED module shall be securely attached to the heatsink with good thermal contact. The diode temperature can be monitored by the negative temperature coefficient (NTC) thermistor connected to Pin 6 and Pin 7.

Note: The heat sink is recommended to be of thermal resistance better than (≤)

$$\frac{T_{op-\max} - T_{Ambient}}{I_{F-\max} \cdot V_{F-\max}}$$ *(°C/W).*

Where $T_{op\text{-}max}$, $I_{F\text{-}max}$, $V_{F\text{-}max}$, $I_{TEC\text{-}max}$, $V_{TEC\text{-}max}$ are the maximum ratings of the operational case temperature, operating current and forward voltage of the diode respectively. Please refer to the specification data sheet or the outgoing report (OGR) for the values.

Example:
Ambient temperature of 35°C, natural convection, and the specified maximum rated case temperature of 40°C, max operating current of 350mA and max forward voltage of 1.5V. Therefore, the thermal resistance of the heat sink is recommended to be ≤ 9.5 °C/W.

Caution: Insufficient heat sinking or poor thermal contact to the heatsink may cause overheating of the TOSA casing. Extended period of operating under this condition may cause permanent damage to the SWIR-SLED.

6. OPERATING INSTRUCTIONS OF SWIR-SLED USING STANDARD COMMERCIAL LD DRIVER

6.1 Description

This section explains the procedure to connect and setup the SWIR-SLED using standard commercial LD driver. Ensure proper ESD precautionary measures are taken before handling the SWIR-SLED and sensitive electronic equipment. Precautionary care has to be taken to avoid continuous viewing of the direct beam. Adequate eye protection against laser radiation should be used while handling and operating the device.

Configure the SWIR-SLED according to the pin assignment of the TOSA as specified (Refer to page 4 of this user manual or pin assignment enclosed in OGR). Attach heat sink to the TOSA for thermal heat dissipation. Secure the pins and the TOSA to ensure good electrical and thermal conductivity.

To solder the leads to the electrical connections on printed circuit board (PCB), it is recommended to take as minimum an amount of time as possible. Do not exceed the soldering heat of 260^{o}C, 10s. We recommend the TOSA to be attached to heat sink during soldering.

Caution: The soldering temperatures apply only to the leads, not to the entire TOSA. The TOSA temperature shall not exceed the maximum temperature of the TOSA (refer to the specification). The TOSA shall not be taken for reflow soldering in the oven.

6.2 Measurement Setup

Typical commercial standard equipment used for measurements:

1. Keithley integrating sphere 2500INT-2-IGAC and 2500 dual photodiode meter
2. Keithley 2420 CW LD driver
3. Keithley 2520 pulse LD driver
4. ANDO A6317B optical spectrum analyzer (OSA)
5. Agilent 33250A function generator
6. Tektronix TDS3052B Oscilloscope
7. New Focus 1414 high-speed photodetector (FC connectorized)
8. Thorlabs F810FC-1550 fiber collimator
9. Single mode fiber (SMF-28) 1m with FC/APC termination
10. Matched high-speed cables with SMA (50 Ohm) connectors
11. BNC cables with 50 Ohm termination

Setup for Measurements:

1. Figure 1a shows the optical power output measurement. Drive the SWIR-SLED using Keithley 2420 CW LD driver for CW operation and Keithley 2520 pulse LD driver for pulse operation. Guide the light directly into the Keithley Integrating sphere 2500INT-2-IGAC and read the photocurrent from Keithley 2500 dual photodiode meter. The optical power should be similar to the report value in the OGR.
2. To check the light source signal, drive the SWIR-SLED using Keithley 2520 pulse LD driver. Guide the collimated light output from the SWIR light source into the New Focus 1414 high-speed photodetector using the Thorlabs F810FC-1550 fiber connector. Connect the monitor output to the input of the Tektronix TDS3052B Oscilloscope using matched high-speed cable. Refer to Figure 1b for the measurement setup. The following parameter can be measured from the oscilloscope:
    - i) Rise time and fall time
    - ii) Pulse width
    - iii) Pulse repetition rate

3. The optical spectrum of the SWIR-SLED can be obtained by driving the SWIR-SLED using Keithley 2420 CW LD driver and guiding the light through SMF-28 into the ANDO A6317B OSA. The measurement setup is shown in Figure 1c.

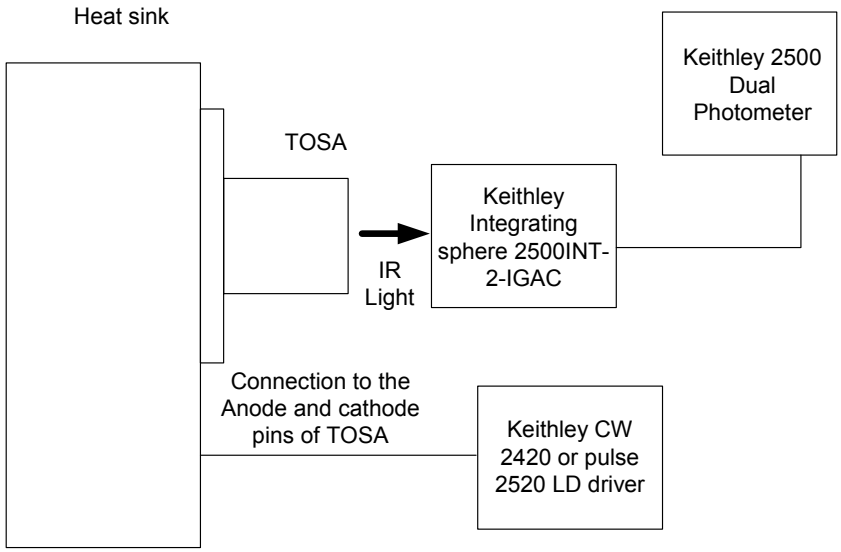


Figure 1a. Optical light source power measurement setup

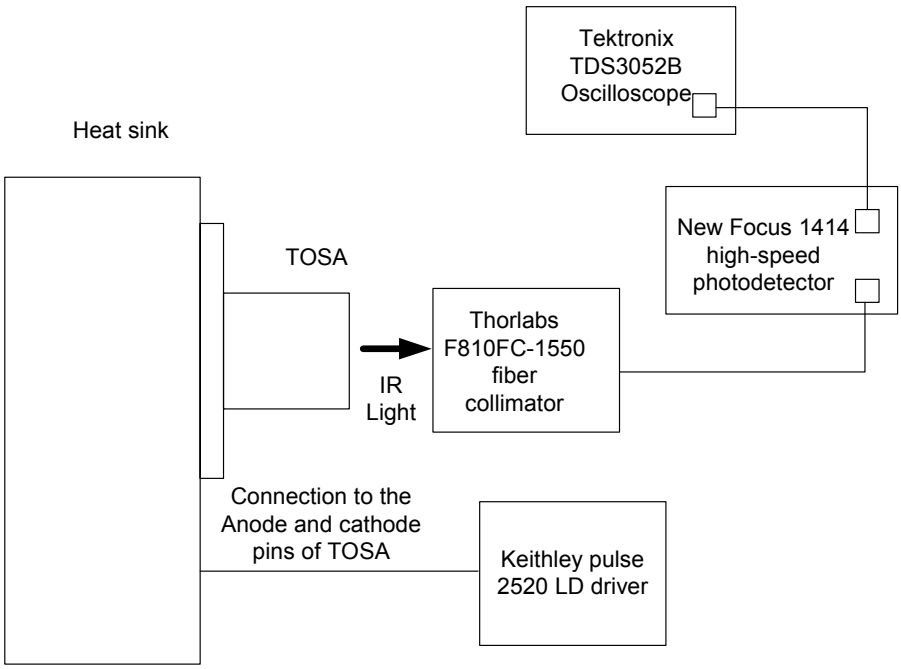


Figure 1b. Optical light source signal measurement setup

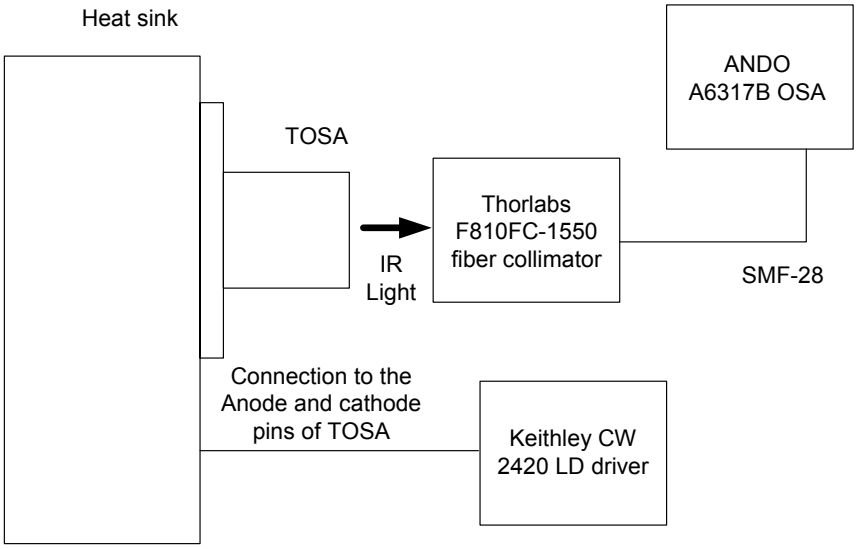


Figure 1c. Optical spectrum measurement setup

7. Operating Instructions of SWIR-SLED using DenseLight Evaluation Board

7.1 Description

DenseLight has designed a DL-CS551502G-L01-Eval evaluation board to offer a platform for customers to evaluate the SWIR-SELD. The board is complete with the essential drive electronics to support a comprehensive range of testing with minimal external electronics instrumentations. The evaluation unit (Figure 2) shows an example of how the SWIR-SLED can be clamped on the evaluation board for thermal dissipation, with short leads for low-inductance high-speed pulse driving of the SLED light output over various range of power levels, pulse width and pulse repetition rate.

Figure 2a. Evaluation board bottom-side where the TO-8 TOSA SWIR light source is mounted

Figure 2b. Evaluation board top side where most of the electronic components are mounted

7.2 Physical Dimensions and Mechanical Specification

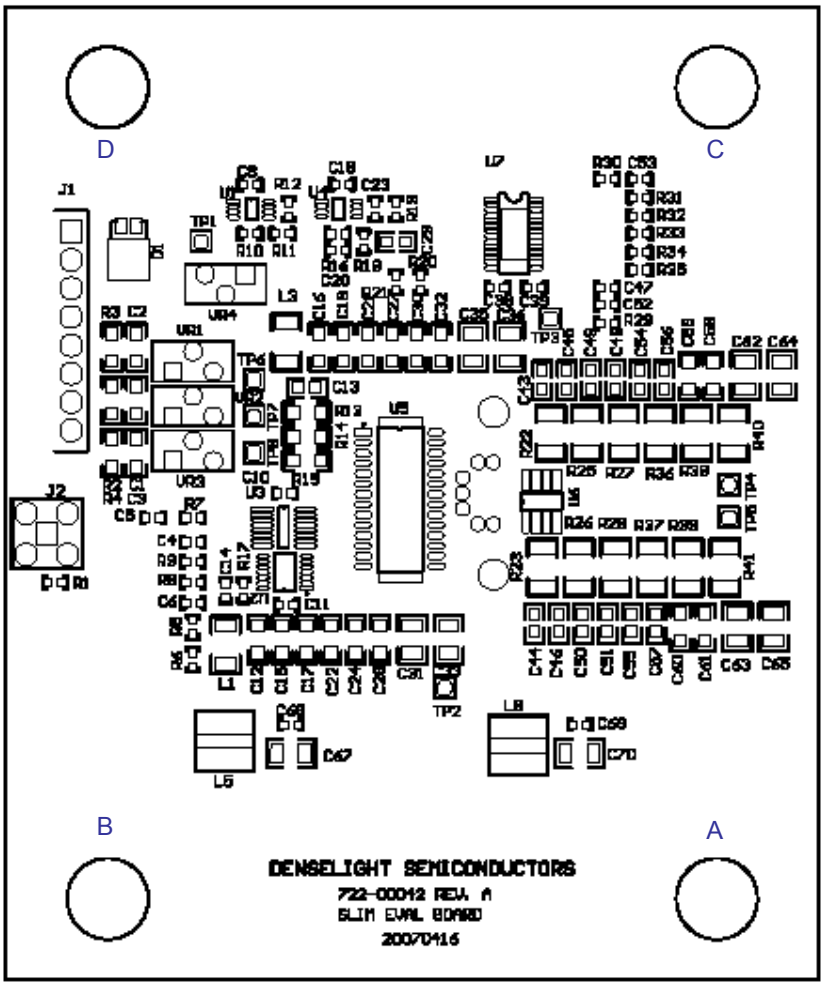


Figure 3a. Top Side Mechanical Layout

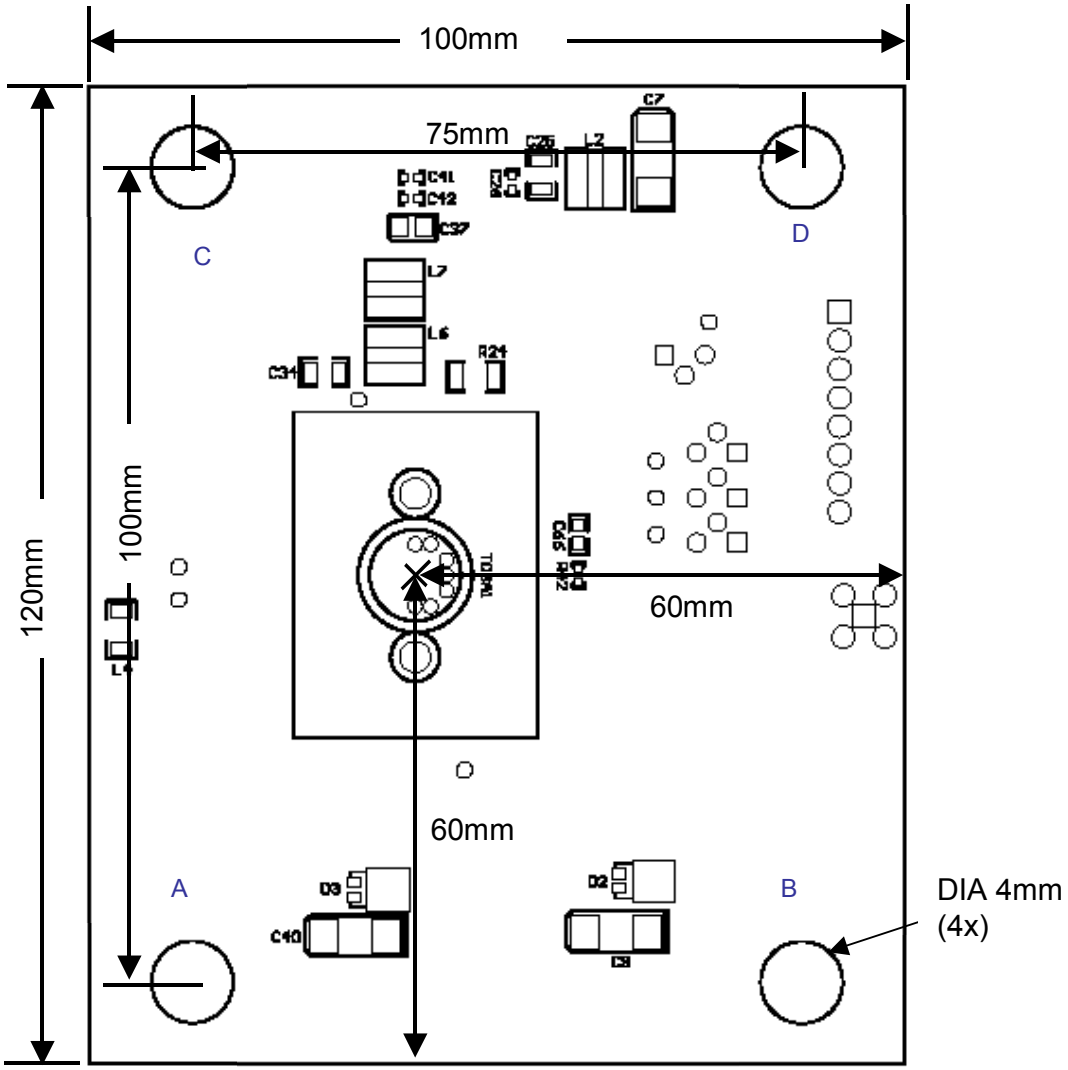


Figure 3b. Bottom Side Mechanical Layout*

* a) Orientation to Top-Side: Reference board mounting holes identifiers A, B, C, D
b) SWIR-SLED light emitting point is identified by "X"

7.3 Pin Assignment and Function

Label	Connector Type	Pin No.	Description
J1	8-pin Header	1	NC
		2	NC
		3	Power supply ground
		4	+7V D.C.
		5	Power supply ground
		6	+9V D.C.
		7	NC
		8	NC
J2	SMA		External Trigger Input (CMOS/TTL compatible)
TP1	Test Point Connector		-
TP2	Test Point Connector		GND
TP3	Test Point Connector		GND
TP4	Test Point Connector		To monitor light source Anode voltage
TP5	Test Point Connector		To monitor light source Cathode voltage
TP6	Test Point Connector		To monitor voltage across VR1 that control the current I_{IBI}, flowing into IBI pin of IXLD02** high-speed LD driver IC that used as a baseline current with respect to I_{IPW} current to compensate for internal delays
TP7	Test Point Connector		To monitor voltage across VR2 that control the current I_{IOP}, flowing into IOP pin of IXLD02 high-speed LD driver IC that used to tune the LD current
TP8	Test Point Connector		To monitor voltage across VR3 that control the current I_{IPW}, flowing into IPW pin of IXLD02 high-speed LD driver IC that used to tune the LD current pulse width

Note:
***Refer to data sheet of IXLD02 at www.directedenergy.com/poudcts/ics.htm*

Caution: Do not apply reverse voltage to pins as this might cause permanent damage to the evaluation board

7.4 Measurement Setup

Equipment used for measurements:

1. Agilent 33250A Function generator
2. Tektronix TDS3052B Oscilloscope
3. Three Topward 3306D DC power supplies
4. Fluke 179 Multimeter
5. New Focus 1414 high-speed photodetector (FC connectorized)
6. Thorlabs F810FC-1550 fiber collimator
7. Keithley Integrating sphere 2500INT-2-IGAC and 2500 dual photodiode meter
8. Single mode fiber (SMF-28) 1m with FC/APC termination
9. Matched high-speed cables with SMA (50 Ohm) connectors
10. BNC cables with 50 Ohm termination

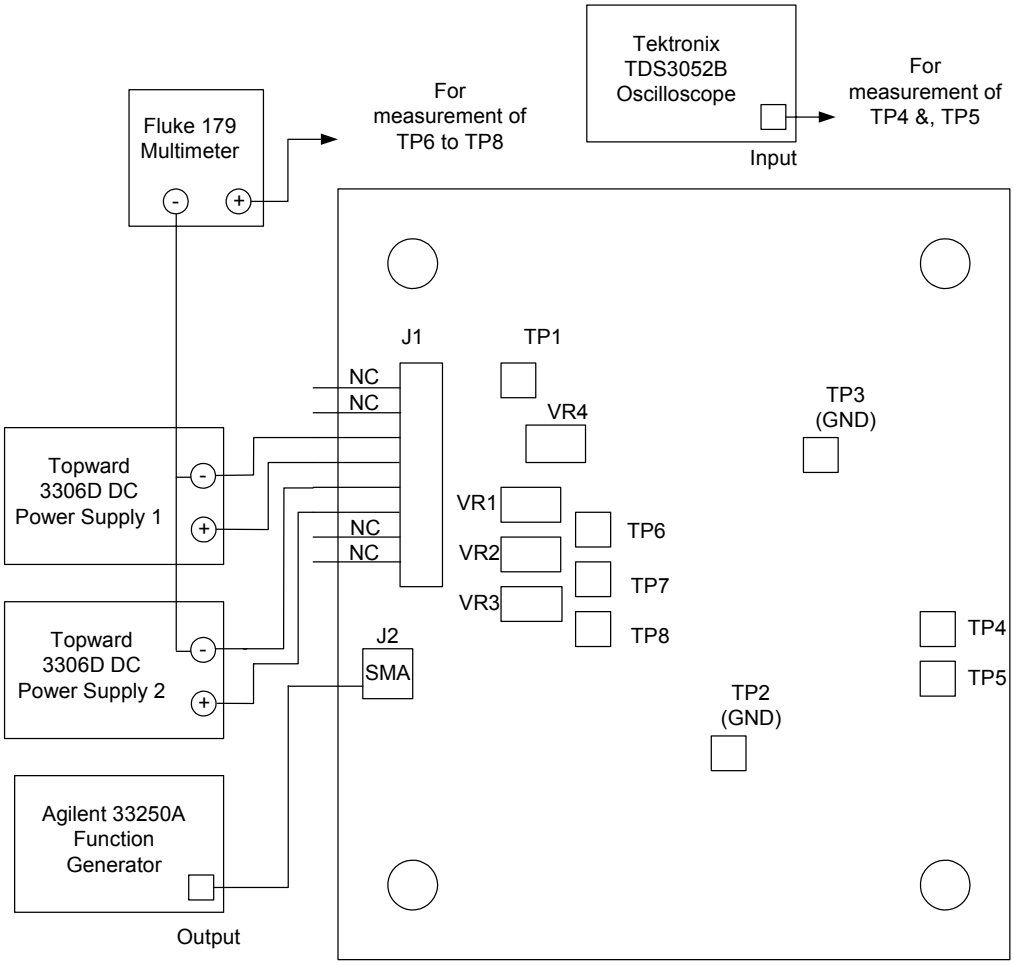


Figure 4a. Power supply connection setup

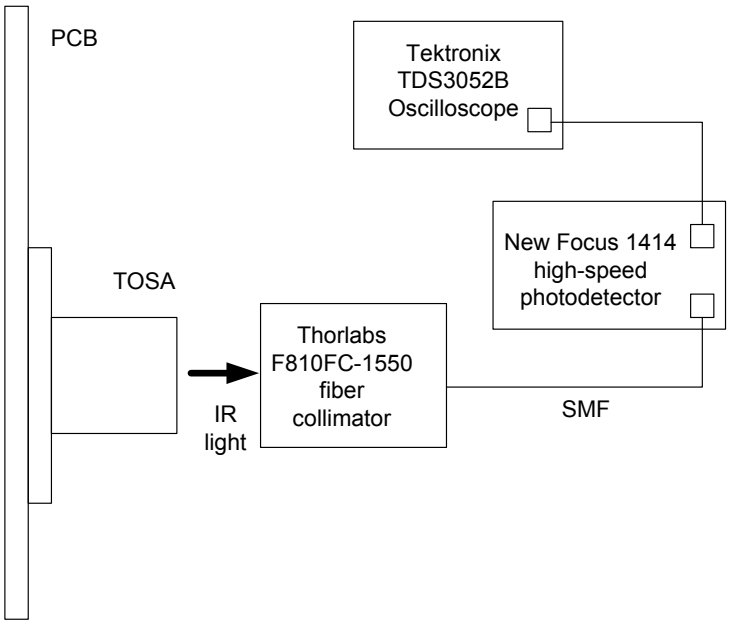


Figure 4b. Optical light source signal measurement setup

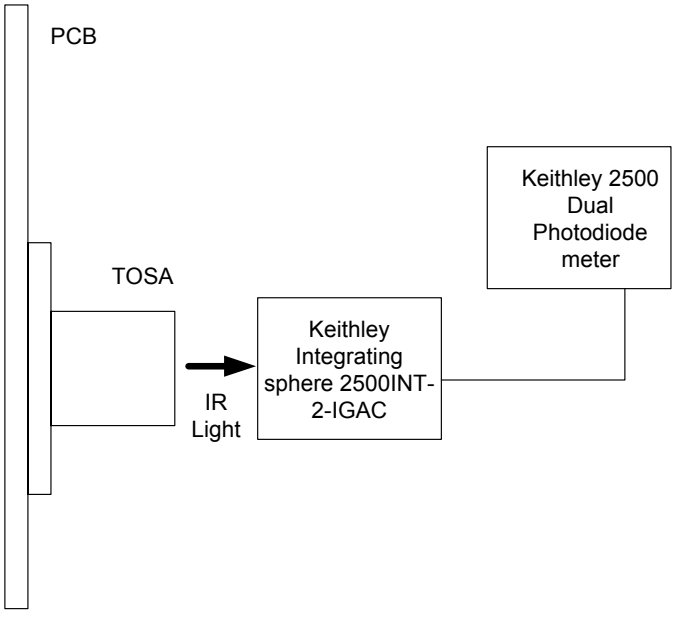


Figure 4c. Optical light source power measurement setup

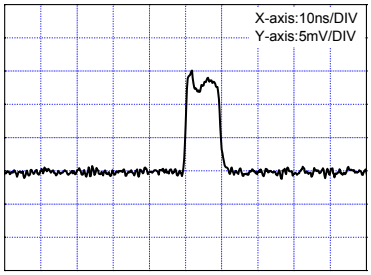
Setup for Measurements:

This section explains the procedure to connect and setup the evaluation board as shown in Figure 4a to 4c. Ensure proper ESD precautionary measures are taken before handling the evaluation board and sensitive electronic equipment. Precautionary care has to be taken to avoid continuous viewing of the direct beam. Adequate eye protection against laser radiation should be used while handling and operating the device.

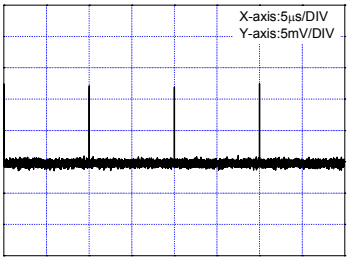
Default Factory Setup:

1. Set Topward 3306D DC Power Supply 1 to 7V output and 1A current limit. Connect J1-3 to the negative terminal and J1-4 to the positive terminal. Turn on the DC Power Supply 1 and this will power up the LD driver of the evaluation board. Measure TP6, TP7 and TP8 using Fluke 179 multimeter. The reading should be similar to the value recorded in OGR attach during shipment.
2. Set Topward 3306D DC power supply 2 to 9V and 1A. Connect J1-5 and J1-6 to the negative and positive terminal. Turn on the DC Power Supply 3. Set the Agilent 33250A function generator with square pulse of amplitude=2Vp-p, frequency=100kHz and Pulse width=500ns (TTL/CMOS logic levels). Connect the signal output from J2 (SMA) to the output of the function generator and this will turn on the IR light source.
3. Guide the collimated light output from the SWIR light source into the New Focus 1414 high-speed photodetector using the Thorlabs F810FC-1550 fiber connector. Connect the monitor output to the input of the Tektronix TDS3052B Oscilloscope using matched high-speed cable. Refer to Figure 4b for the measurement setup. Measure the following parameter from the oscilloscope:
   iv) Rise time and fall time
   v) Pulse width
   vi) Pulse repetition rate

   A typical trace of pulse is shown in Figure 5. Measure TP6, TP7 and TP8 using Fluke 179 multimeter. The reading should be similar to the value recorded in OGR attached during shipment. Fine-tune the pulse width by adjusting the VR3 if it varies from the setting. To measure the voltage across the SWIR light source, obtain the voltage difference between TP4 (TP3 as GND) and TP5 (TP2 as GND) using Tektronix TDS3052B Oscilloscope. The reading should be ~2 to 3V.
4. Refer to Figure 4c for the measurement setup of optical power output. Guide the light directly into the Keithley Integrating sphere 2500INT-2-IGAC and read the photocurrent from Keithley 2500 dual photodiode meter. The peak pulse power is >150mW.



(a)



(b)

Figure 5. Scope trace of (a) Single pulse (b) Pulse train, with pulse width=10ns and repetition rate =100kHz.

7.5 LD Current Pulse Width Tuning:

The pulse width of the current that drive the SWIR light source can be tuned via variable resistors VR1 and VR3. VR1 controls the current IIBI, flowing into IBI pin of IXLD02 high-speed LD driver IC that is used as a baseline current with respect to IIPW current to compensate for internal delays. Whereas, VR3 controls the current IIPW, flowing into IPW pin of IXLD02 high speed LD driver IC that is used to tune the SWIR light source current pulse width. Turning the VR1 and VR3 in clockwise direction will reduce the IIBI and IIPW, while anti-clockwise will increase both values. The voltage across VR1 and VR3 can be monitored via TP6 and TP8 respectively. The value of IIBI should be higher than IIPI. If IIPW=IIBI, the pulse width is 0. As IIPW approaches IIBI but less than IIBI, the pulse width becomes smaller. Figure 6 illustrates the relationship of current pulse width tPW versus IIPW with respect to IIBI.

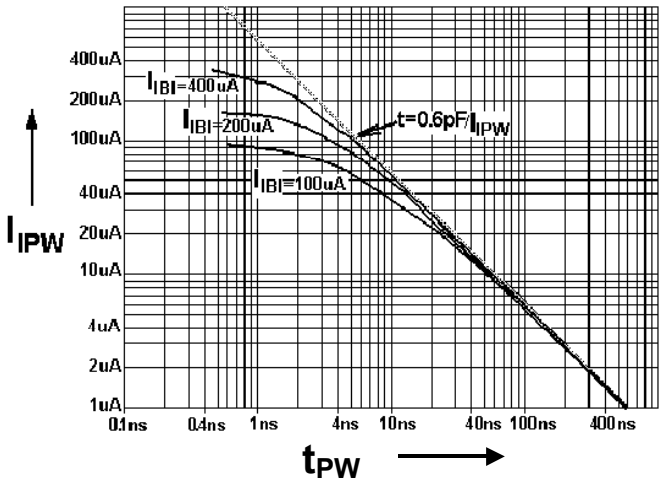


Figure 6. Current pulse width versus IPW current (Abstracted from page 5 of IXL02 Ultra high-speed laser diode driver IC specification from Directed Energy Inc)

7.6 LD current tuning:

The output current that drive the SWIR light source can be tuned via variable resistors VR2. VR2 controls the current IIOP, flowing into IOP pin of IXLD02 high-speed LD driver IC that is used to tune the driving current. The voltage across VR2 can be monitored via TP7, while the voltage across the IR light source can be obtained from the measurement of voltage difference between TP4 (TP3 as GND) and TP5 (TP2 as GND) using Tektronix TDS3052B Oscilloscope.

8. More Information and Technical Support

Please contact DenseLight Semiconductor Pte Ltd for further information and technical support.

9. Revision Control

Authorized Personnel	Rev	Description of Change	Date
OTK	A	Initial: Production Release	8 September 2007